RF Linearity Performance Potential of Short-Channel Graphene Field-Effect Transistors

Ahsan Ul Alam, Kyle David Holland, Michael Wong, Sabbir Ahmed, Diego Kienle, and Mani Vaidyanathan, *Member, IEEE*

***Abstract*—The radio-frequency (RF) linearity performance potential of short-channel graphene field-effect transistors (GFETs) is assessed by using a nonlinear small-signal circuit model under the first approximation of ballistic transport. An intrinsic GFET is examined to reveal the key features of GFET linearity, and extrinsic parasitics are then included to assess the overall RF linearity. It is shown that short-channel GFETs can be expected to have a signature behavior versus gate bias that includes a constant-linearity region at low gate bias, sweet spots of high linearity before and after the gate bias for peak cutoff frequency, and poor linearity at the gate bias corresponding to the peak cutoff frequency. It is otherwise found that a GFET offers overall linearity that is comparable to a MOSFET and a CNFET, with the exception that the amount of intermodulation distortion in a GFET is dominated by the drain-injected carriers, a unique outcome of graphene's lack of a bandgap. Qualitative agreement with experiment in the signature behavior of GFET linearity supports the approach and conclusions.**

***Index Terms*—Contact resistance, device modeling, device physics, FET devices and circuits, FET modeling, GFET, graphene, graphene transistor, harmonic balance, intermodulation distortion, linearity, nanoelectronics, nonlinear device modeling, radio-frequency performance, solid state devices, third-order input-intercept point, transistor modeling.**

I. Introduction

GRAPHENE is a two-dimensional sheet of carbon, in which the atoms are arranged in a honeycomb lattice. The unique electrical and physical properties of graphene have sparked much interest in determining its potential uses in electronics. Although the lack of a bandgap has been problematic for the use of graphene in digital applications, the high values of unity-current-gain frequency f_T and unity-power-gain frequency $f_{\max}$, combined with a high carrier mobility, continue to make graphene a promising candidate for analog high-frequency, or radio-frequency (RF), electronics. A key figure-of-merit for RF applications is linearity, which measures the degree of distortion generated by the nonlinear mixing of the input signal with jammers. This paper probes the performance potential of graphene in terms of RF linearity.

The strong interest in graphene has resulted in many theoretical and experimental studies on graphene field-effect transistors (GFETs). These studies have largely focused on cut-off frequencies [1]–[3], mobility [4]–[6], the effect of the lack of a bandgap [7], and ways to introduce a bandgap to improve performance [8]–[10]. GFETs operating at promisingly high frequencies have already been demonstrated [11]. Furthermore, great progress has been made in the pursuit of graphene-based integrated circuits [12]–[14].

On the topic of graphene linearity, however, there has been limited experimental work, which can be summarized as follows. Wang *et al.*[15] investigated the linearity of a 2-μm long single transistor RF mixer at 10 MHz and reported a third-order input-intercept-point (IIP3) of $\sim$ 13.8 dBm; however, the reported conversion loss was between 30 to 40 dB. Habibpour *et al.*[16] reported a mixer based on a 500-nm long multichannel GFET operating at 30 GHz, with IIP3 values as high as 12.8 dBm and a conversion loss of 19 dB. Andersson *et al.*[17] reported the linearity of subharmonic mixers based on resistive GFETs having a channel length of 1 μm; they obtained an IIP3 of 4.9 dBm and a conversion loss of 20–22 dB. The shortest channel GFET investigated for RF linearity thus far is a 250-nm epitaxially grown graphene FET used as a mixer, reported by Moon *et al.*[18] with an IIP3 of $\sim$22 dBm and conversion loss $>$15 dB; they also reported a similar but longer channel (2 μm) device with higher IIP3 ($\sim$27 dBm) and conversion loss of 10 dB. Madan *et al.*studied the linearity of an RF mixer [19] and LNA [20] based on a 750-nm long graphene FET and reported third-order output-intercept point (OIP3) values in the range of 19 dBm at an operating frequency of 2 GHz; the gain of the LNA for a 50-Ω load termination was -5 dB. Jenkins *et al.*[21] also reported relatively good linearity for graphene FETs containing channels grown both by chemical vapor deposition and epitaxy and having lengths above 500 nm, with IIP3 values as high as 20 dBm but a power gain of $<$15 dB for a 50-Ω load at 300 MHz. In a recent study, Han *et al.*[14] fabricated a graphene RF receiver integrated circuit with promising linearity figures of merit. Operating at a frequency of 4.3 GHz, the receiver produced very low RF harmonic distortion, with the output power of the second harmonic recorded to be 30 dB lower than the output power of the fundamental tone for an input power of 0 dBm; the conversion loss of the receiver was 10 dB.

Common trends in the results cited above are a long channel length ($>$250 nm) for the devices and promising values of IIP3

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A. U. Alam, K. D. Holland, M. Wong, S. Ahmed, and M. Vaidyanathan are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2V4, Canada (e-mail: maniv@ece.ualberta.ca).

D. Kienle is with the Theoretische Physik I, Universität Bayreuth, 95440 Bayreuth, Germany.

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that are accompanied by very low power gains. Further investigation is thus necessary to fully understand the RF linearity potential of GFETs, particularly the linearity that could be realized at short channel lengths.

Given the present difficulty of fabricating GFETs with channel lengths at or below those for current CMOS technology nodes, studying the linearity of GFETs with short channels, i.e., $\lesssim$20 nm, which is 10 to 100 times smaller than the reported experimental devices cited above, calls for a modeling approach. To date, there have been only a few modeling studies that explore GFET linearity, and these have also focused on longer channel devices ($\geq$440 nm). Chauhan *et al.*[22] used a semi-classical model incorporating the effects of inelastic phonon scattering and reported "excellent" linearity; however, the claim was based solely on the fact that the transconductance of their (1-μm long) GFET was observed to remain nearly constant over a wide range of gate bias. Parrish *et al.*[23] performed an analytical study that shows that the contact resistances can severely degrade GFET transconductance linearity; working on a 2.4-μm long device, they showed that the IIP3 of a GFET can improve by as much as 17 dB if the contact resistances are made small enough to be neglected. Very recently, Rodriguez *et al.*[24] used a static (low-frequency) analytical model to investigate the transconductance linearity of a 440-nm long GFET and reported a peak IIP3 value of 13.8 dBm. None of these modeling studies accounted for all sources of nonlinearity relevant for RF performance. In particular, both transport *and* capacitive nonlinearities can be expected to play a role [25]. A detailed and more comprehensive study of the RF linearity mechanisms in short-channel GFETs is thus warranted.

In this work, we provide insight into the linearity mechanisms of an 18-nm GFET, chosen for demonstration purposes and representative of current CMOS technology nodes [26]. As in [27], we assume ballistic transport, a reasonable first approximation for graphene at small channel lengths ($\lesssim$20 nm) for the purposes of assessing performance potential, especially since the reported electron mean-free path in graphene is much larger ($\gtrsim$100 nm) [28]. We also consider a doped MOSFET-like device, as done in recent studies to assess the performance potential of carbon-based electronics [27], [29]; short-channel MOSFET-like devices can be expected to outperform the long-channel Schottky-barrier devices prevalent today [30] and are a suitable choice to gauge performance potential. Although graphene's ambipolar transport has been exploited in RF applications [15], [19], in this study, we consider a unipolar configuration in which the device is biased away from the point of minimum conduction.

We start our analysis by using an already developed nonlinear small-signal circuit [25]. The intrinsic components of the circuit are first extracted based on a modified top-of-the-barrier model (MTBM) [31]. The MTBM is an extension of the conventional top-of-the-barrier model [27], [29], with additional features to account for physical effects arising from the lack of a bandgap in graphene; for further details, the reader is referred to [31]. The external parasitics are then calculated with the aid of COMSOL [32] and added to obtain a complete extrinsic nonlinear circuit, an approach which has already been shown [31] to capture the nonlinear voltage dependencies of key device parameters determined from a more detailed simulator [7]. The Harmonic Balance solver in Microwave Office (MWO) [33] is then used to simulate the developed nonlinear circuit.

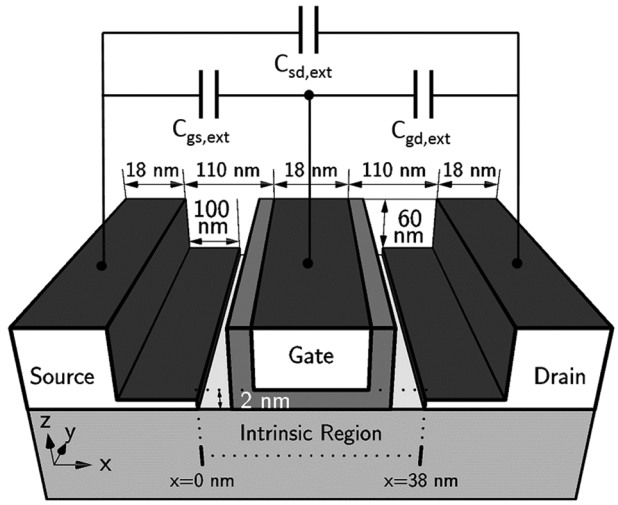

Fig. 1. Schematic of the GFET used in this paper. The dotted intrinsic region is modeled using a modified top-of-the-barrier method [31]. The external parasitic capacitances used to model the extrinsic device are shown at the top of the schematic.

Based on an examination of IIP3 values for intermodulation distortion under a two-tone input, our study reveals that GFETs offer linearity performance comparable to MOSFETs and CNFETs. They also exhibit a unique linearity signature, the features of which can be explained by an in-depth examination of the sources of nonlinearity in the device. We further find that, unlike MOSFETs and CNFETs, carrier injection from the drain dominates the nonlinear behavior of GFETs. We also examine the effects of drain bias, load resistance, and external parasitics. Finally, we perform a qualitative comparison with recent experiments [21] to validate our work.

Section II of this paper outlines the device structure and simulation methodologies. The results of our simulation are presented and discussed in Section III, and a qualitative comparison of these results with experiment is provided in Section IV. The conclusions of our study are summarized in Section V.

II. Approach

A. Device Structure

Fig. 1 shows the schematic of the GFET under investigation, with key device dimensions marked. The dotted region indicates the intrinsic portion of the device. The gate oxide is a 2-nm layer of Al_2O_3 (with a relative permittivity $\epsilon_r = 9.8$). Al_2O_3 has been demonstrated as a promising high-k dielectric suitable for graphene in recent experiments [34], [35]. The channel is intrinsic graphene, while the source and drain regions are n-doped, with an effective doping concentration of $N_D = 1.9 \times 10^{17}$ m^{-2}. The source and drain geometries are symmetric with respect to the channel/gate regions.

Fig. 2 plots the current-voltage characteristics of the GFET calculated using the MTBM [31] and a fully quantum-mechanical solver based on NEGF [7]. The results from the MTBM are in excellent agreement with those from NEGF, except for the

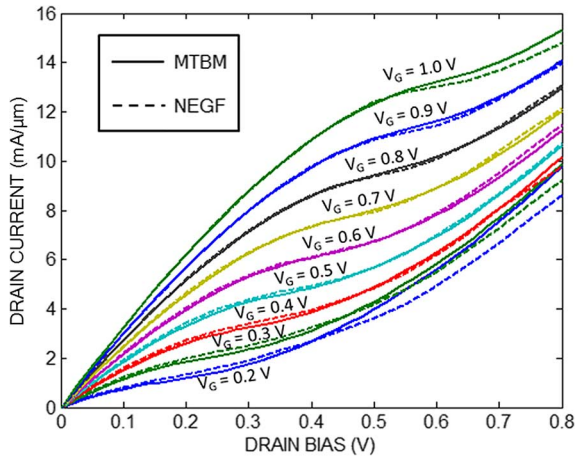

Fig. 2. Simulated current-voltage characteristics of the GFET under investigation from MTBM and NEGF.

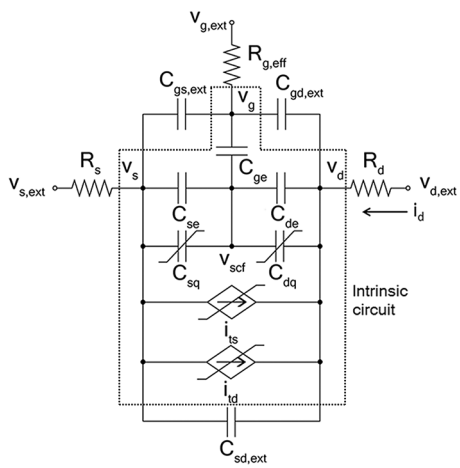

Fig. 3. Complete nonlinear small-signal equivalent circuit of a ballistic GFET.

combination of very low gate bias ($V_G \leq 0.2$ V) and high drain bias ($V_D \geq 0.5$ V); however, this study focuses on operation at a drain bias of 0.5 V, where the MTBM clearly provides a sufficiently accurate picture of device behavior at all gate biases. It should also be noted that Fig. 2 shows drain current values for an intrinsic device considering ballistic transport, and therefore depicts a "best-case scenario" for current. In an actual device, the measured current density would be significantly reduced due to contact resistances, scattering due to phonons and interface states, and other nonidealities. Other important parameters such as transconductance g_m, output conductance g_o (or g_{ds}), and unity-current-gain (cutoff) frequency f_T of the device were reported in [31]; plots of these quantities versus gate bias are also available in figures (4 and 11) discussed further below.

B. Intrinsic Equivalent Circuit

Our focus in this work is the small-signal nonlinear operation of GFETs. We hence use Taylor-series expansions for all the components in the small-signal equivalent circuit. The coefficients of the series are specified by derivatives [evaluated at corresponding bias (dc operating) point] of the charge-voltage and current-voltage relationships from the MTBM [31]. The dotted portion of Fig. 3 represents the intrinsic nonlinear small-signal equivalent circuit, where the elements are as follows: C_{ge}, C_{se}, and C_{de} are the linear electrostatic capacitances of the GFET; C_{sq} and C_{dq} are the nonlinear source and drain quantum capacitances; and i_{ts} and i_{td} are the nonlinear current sources modeling the quasi-static transport currents of the device. The interested reader can find further details on these elements in [29]. Although [29] is developed for CNFETs, the methodology can, in principle, be used to model any ballistic MOSFET-like device. By accounting for both band-to-band tunneling and the unique density of states of graphene, as done in the MTBM, we can adapt this method to model GFETs [31].

Each of the nonlinear components are represented by a Taylor-series expansion up to third order, which is sufficient to capture their nonlinearity under small perturbation [36]:

$$q_{sq} = C_{sq1}(v_s - v_{scf}) + C_{sq2}(v_s - v_{scf})^2 + C_{sq3}(v_s - v_{scf})^3 \quad (1)$$

$$q_{dq} = C_{dq1}(v_d - v_{scf}) + C_{dq2}(v_d - v_{scf})^2 + C_{dq3}(v_d - v_{scf})^3 \quad (2)$$

$$i_{ts} = g_{sq1}(v_s - v_{scf}) + g_{sq2}(v_s - v_{scf})^2 + g_{sq3}(v_s - v_{scf})^3 \quad (3)$$

$$i_{td} = g_{dq1}(v_d - v_{scf}) + g_{dq2}(v_d - v_{scf})^2 + g_{dq3}(v_d - v_{scf})^3 \quad (4)$$

where q_{sq} and q_{dq} are the small-signal (ac) parts of the charges held by the quantum capacitances C_{sq} and C_{dq}, respectively; v_s and v_d are the small-signal parts of the source and drain voltages, respectively; and v_{scf} is the small-signal part of the (self-consistent) channel potential. The steps described in [25] were followed to determine the values of the linear and nonlinear components from the MTBM [31].

C. Extrinsic Equivalent Circuit

The performance of a practical GFET is also impacted by the parasitic elements in the device due to the metallic contacts at the gate, source, and drain. In order to fully assess the linearity of these devices, the effects of these parasitics must be incorporated. We therefore add the extrinsic capacitances $C_{gs,ext}$, $C_{gd,ext}$, and $C_{sd,ext}$, labeled in Fig. 1 along with the contact resistances of the gate, drain, and source, $R_{g,eff}$, R_s, and R_d, respectively. All the parasitic components were calculated following the method described in [25]with the aid of COMSOL [32], and by using the contact dimensions specified below in Section III-D. The resulting extrinsic nonlinear small-signal equivalent circuit is the overall circuit in Fig. 3, where v_g, v_s, and v_d are the internal node voltages of the GFET and $v_{g,ext}$, $v_{s,ext}$, and $v_{d,ext}$ are the external terminal voltages of the overall device. The component values (both intrinsic and extrinsic) are listed in Table II in Section III-D for the device under investigation.

III. Results and Discussion

We used the Harmonic Balance solver in MWO [33] to simulate the nonlinear small-signal equivalent circuit, and we extracted the IIP3 corresponding to the mixing frequency $2f_1 - f_2$, under excitation from two input tones at the fundamental frequencies f_1 and f_2, as the small-signal linearity figure of

merit of the device. The transistor was deployed in a simple common-source configuration. The load and source impedances were set at 50 Ω, the usual characteristic impedance for RF applications. A two-tone source with an impedance of 50 Ω and an operating frequency of 24 GHz—which is a frequency of interest in RF electronics according to the 2012 ITRS [26]—and a difference of 100 MHz between the two tones was used ($f_1 = 24$ GHz, $f_2 = 24.1$ GHz). The input power was swept from -50 dBm to -40 dBm to keep the perturbation sufficiently small. The source was grounded, the drain bias was fixed at $V_D = 0.5$ V, and the gate bias was varied over a wide range, from 0 to 1 V (except for the results in Figs. 6 and 10, where the upper limits are 1.2 V and 1.4 V, respectively, and Fig. 19, where the range is from -0.1 V to 1.5 V, to aid the discussion).

The IIP3 values in this paper are quoted in terms of the corresponding available power from the source, $P_{\mathrm{av,s}}$. Due to the large mismatch at the input, it should be noted that a significant amount of reflection loss occurs at the input of the device, which means the IIP3 values quoted in terms of $P_{\mathrm{av,s}}$ will be significantly higher than the actual input power P_{in} at the intercept point. However, the aim of this study is to examine the *qualitative* nature of a GFET's RF linearity and to investigate the mechanisms behind high-frequency distortion in this device. Our use of $P_{\mathrm{av,s}}$ as the reference for quoting IIP3 is hence sufficient for the qualitative purposes of this study. In order to remain in the small-signal regime, $P_{\mathrm{av,s}}$ was kept small (-50 to -40 dBm). In this range, the IM3-$P_{\mathrm{av,s}}$ relation showed a slope of three as expected, with no variation.

A. Key Features of GFET Linearity

To reveal the key features of GFET linearity, we first investigated the intrinsic RF linearity of a GFET, i.e., the linearity determined by the dotted portion of Fig. 3 and excluding external parasitics. The resulting IIP3 was plotted against variations in gate bias and is shown in Fig. 4. The IIP3 curve has a very distinct shape (signature), with a constant linearity region (region 1), two sharp peaks at points 2 and 4, and a large dip around point 3. The presence of the peaks at points 2 and 4 mean that bias sweet spots may exist where a GFET will behave very linearly. Fig. 4 also shows the unity-current-gain frequency f_T versus gate bias. f_T is defined as the operating frequency at which the small-signal current gain of the transistor in a common-source configuration drops to unity. It is a commonly used figure-of-merit in evaluating the amplification ability of a transistor. Note that the peak f_T coincides with point 3, which means the GFET is most nonlinear at peak f_T.

1) Constant IIP3 Region (Region 1): From the small-signal equivalent circuit in Fig. 3, it is clear that the distortion in a GFET arises from the nonlinear quantum capacitances and current sources, labeled C_{sq}, C_{dq}, i_{ts}, and i_{td}. More precisely, intermodulation distortion at the third-order mixing frequency $2f_1 - f_2$, which is of principal interest in this paper, arises due to the nonzero second- and third-order coefficients of the corresponding Taylor series expansions (1)–(4) for these elements; the second-order coefficients contribute by creating second-order distortion and then re-mixing it with the fundamental frequencies, and the third-order terms contribute by directly mixing the fundamental frequencies. We hence focus our attention on the behavior of both the second- and third-order coefficients.

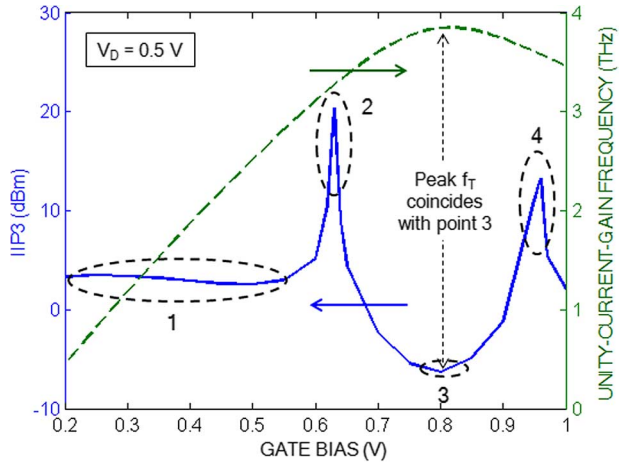

Fig. 4. Simulation results for intrinsic IIP3 and unity-current-gain frequency f_T versus gate bias for the GFET under investigation.

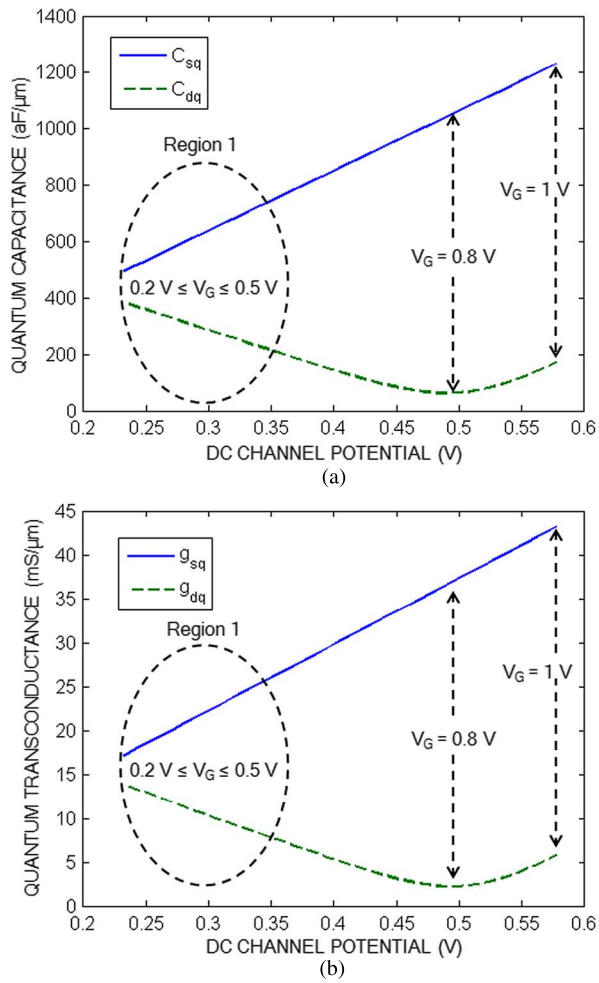

Fig. 5. Simulated (a) quantum capacitance and (b) transconductance versus the dc part of the channel potential for the GFET under investigation. The gate bias voltages for a few points are indicated for reference.

Fig. 5 plots the quantum capacitances $(C_{\mathrm{sq}}, C_{\mathrm{dq}})$ and quantum transconductances $(g_{\mathrm{sq}}, g_{\mathrm{dq}})$ with respect to the bias (dc) part of the channel potential V_{SCF}, where the capacitances

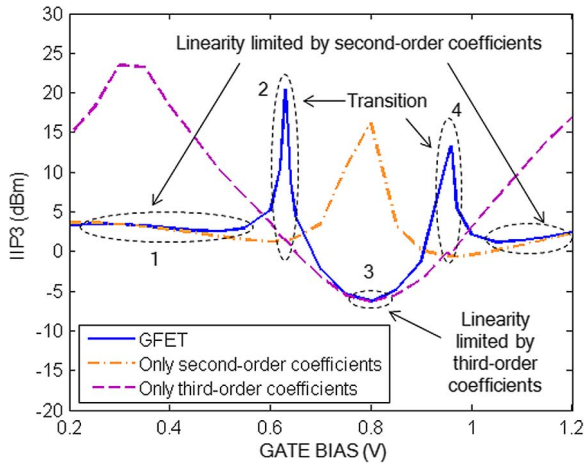

Fig. 6. Effects of the second and third-order coefficients on the overall linearity of the GFET from simulation.

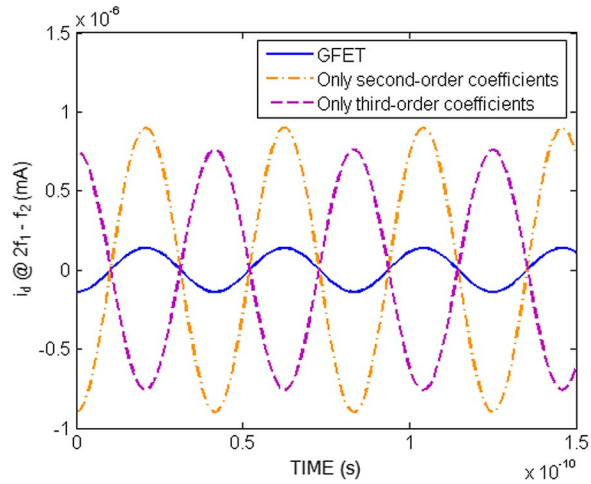

Fig. 7. Distortion components at $2f_1 - f_2$ in the simulated drain current $i_{\rm d}$ at a gate bias of 0.63 V (point 2 in Fig. 6). A destructive combination of the distortion from the two types of sources results in a diminished overall distortion.

are defined as the derivatives of the source- and drain-injected charge with respect to the channel potential, respectively, and the quantum transconductances are similarly defined but involving derivatives of currents [29]. The values of gate bias voltage V_G that apply are also indicated for a few points on the plots. Since the curves were obtained with constant source and drain voltages, then by definition, the values of the capacitances $(C_{\rm sq}, C_{\rm dq})$ and transconductances $(g_{\rm sq}, g_{\rm dq})$ on the plots are the *first*-order coefficients $C_{\rm sq1}$, $C_{\rm dq1}$, $g_{\rm sq1}$, and $g_{\rm dq1}$ appearing in (1)–(4). The second- and third-order coefficients in (1)–(4) are therefore determined by the first and second derivatives of the curves in Fig. 5. It can be seen that in region 1 ($0.2\ {\rm V} \leq V_G \leq 0.5\ {\rm V}$), the curves vary linearly with voltage, which means that the third-order coefficients (determined by the second derivatives) are almost zero, while the second-order coefficients (first derivatives) are constant, thereby yielding a steady amount of distortion in the device over region 1. The linear behavior of the capacitances and transconductances in region 1, and hence the constant IIP3 in region 1, arise from the linear density of states (DOS) of graphene; the connection between the DOS and the expected behavior is explained for $C_{\rm dq}$ and $g_{\rm dq}$ when discussing Fig. 8, and similar reasoning applies for $C_{\rm sq}$ and $g_{\rm sq}$.

2) Sharp Peaks at Points 2 and 4: The distortion in a GFET can arise from multiple sources, and the distortion generated from these sources can act upon each other constructively or destructively. In the discussion to follow, we show that the peaks at points 2 and 4 arise due to the destructive combination of distortion from two different sources. Using appropriate biasing, it may therefore be possible to make the GFET behave very linearly.

To identify how the GFET's linearity is affected by the contributions from the second and third-order coefficients in (1)–(4), we turn them on and off selectively in the intrinsic equivalent circuit of Fig. 3. Fig. 6 shows the IIP3 of the GFET due to the two types of coefficients.

It is evident that over particular bias points, the GFET linearity is determined by one of the two types of coefficients. At low and high gate biases ($V_G < 0.6$ V and $V_G > 1.0$ V),

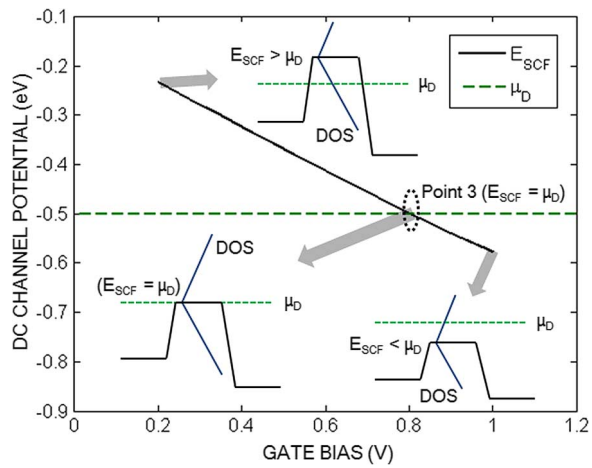

Fig. 8. The dc part of the simulated channel potential $E_{\rm SCF} = -qV_{\rm SCF}$ versus gate bias. The drain Fermi level μ_D (fixed by the constant drain voltage of 0.5 V) is also shown. The source Fermi level μ_S (not shown) is taken to be the reference ($\mu_{\rm S} = 0$ eV).

the device linearity is limited by the distortion generated by the second-order coefficients. However, for the moderate bias range $0.7\ {\rm V} \leq V_G \leq 0.9\ {\rm V}$, the device linearity is limited by distortion generated by the third-order coefficients. The peaks at points 2 and 4 appear when the device linearity mechanism switches from one type to the other. These results strongly suggest that at the transition regions, distortion contributions from the two mechanisms are combining in such a way that they cancel each other, making the device extremely linear. To illustrate the cancellation, MWO was used to generate the distortion components of the small-signal output current $i_{\rm d}$, at the mixing frequency $2f_1 - f_2$, in the transition regions; Fig. 7 shows the results at a gate bias of 0.63 V (point 2). It is seen that the distortion due to the two mechanisms (second and third-order coefficients) are indeed 180° out of phase. Similar behavior is observed at the gate bias of 0.96 V (point 4).

3) Dip at Point 3: The dip in GFET IIP3 at point 3 occurs where device linearity is limited by the third-order coefficients, as shown by the results in Fig. 6. An inspection of Fig. 5 shows

that the source components $C_{\rm sq}$ and $g_{\rm sq}$ [solid lines in parts (a) and (b) of Fig. 5] behave linearly over all gate biases of interest, meaning their third-order coefficients (determined by the second derivatives) are zero, but the drain components $C_{\rm dq}$ and $g_{\rm dq}$ [dashed lines in parts (a) and (b) of Fig. 5] both show minima at point 3 ($V_G = 0.8$ V), which leads to large third-order coefficients (determined by the second derivatives). The nonlinear elements $C_{\rm dq}$ and $g_{\rm dq}$ associated with the drain can hence be expected to contribute substantial distortion around point 3, which limits the device linearity, as illustrated in Fig. 6. The origin of the minima in $C_{\rm dq}$ and $g_{\rm dq}$ can be explained by observing what happens to the drain transport in this bias region.

Fig. 8 shows the dc channel potential $E_{\rm SCF} = -qV_{\rm SCF}$, equivalent to the position of the Dirac point in the channel of a GFET, as a function of gate bias. As illustrated, the channel potential (Dirac point) decreases with an increasing gate bias and crosses the drain Fermi level $\mu_D = -0.5$ eV at point 3, i.e., for $V_G = 0.8$ V. The insets in Fig. 8 are provided as visualization aids and show the position of the Dirac point and channel DOS with respect to the drain Fermi level at a few gate biases. It can be seen that at lower gate biases ($V_G < 0.8$ V), μ_D is positioned below the channel potential and a large number of states are available in the channel at the drain Fermi level. As the gate bias increases, the available DOS at μ_D starts to decrease and becomes zero at point 3, where the channel Dirac point aligns with the drain Fermi level ($E_{\rm SCF} = \mu_D$). Beyond point 3 ($V_G > 0.8$ V), μ_D is positioned above the channel potential, and the number of states available at the drain Fermi level increases with gate bias. Since the drain quantum capacitance $C_{\rm dq}$ depends directly on the available DOS at the drain Fermi level [37], it follows the same trend, i.e., $C_{\rm dq}$ decreases linearly with gate bias before reaching point 3, becomes a minimum at point 3, and increases linearly after point 3. The (energy-independent) constant velocity of electrons (and holes) in graphene means that $i_{\rm td}$ in Fig. 3 and its first derivative $g_{\rm dq}$ behave in the same way as q_{dq} and its first derivative $C_{\rm dq}$, respectively, which can be discerned by their governing equations [29]. Thus, both $C_{\rm dq}$ and $q_{\rm dq}$ show minima at $V_G = 0.8$ V (Fig. 5), i.e., at point 3 (Fig. 6).

B. Drain Dominance in GFET Linearity

To further investigate the role of the drain in determining the linearity of a GFET, we selectively turned on and off the distortions from the source and drain components, by setting the appropriate higher-order coefficients in (1)–(4) to zero. The results are shown in Fig. 9. For all gate voltages, the linearity of the device is found to be dominated by distortion coming from the drain. This result is significantly different from a conventional field-effect transistor in which the channel material has a finite bandgap (MOSFET or CNFET), where the distortion primarily comes from the source components [25]. The reason behind this unique drain dependency of the GFET linearity is two-fold:

i) The zero bandgap of graphene means that the drain always contributes to the transport. Consequently, the drain quantum capacitance and quantum transconductance of the GFET [dashed curves in Figs. 5(a) and 5(b)] are always large enough to impact the overall device behavior.

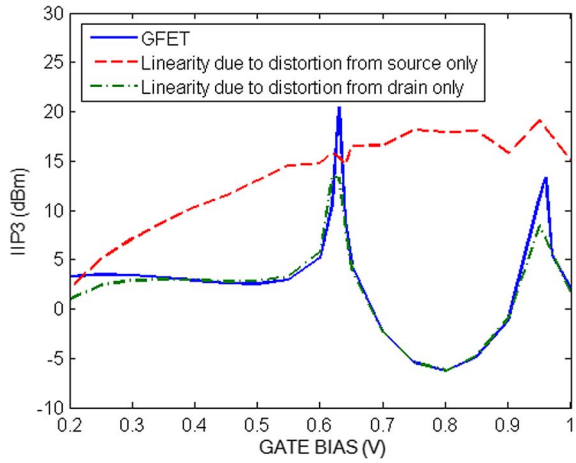

Fig. 9. Effect of distortion from the source and drain on simulated IIP3. Linearity due only to the source was found by setting the higher-order coefficients in (2) and (4) to zero; similarly, linearity due only to the drain was found by setting the higher-order coefficients in (1) and (3) to zero.

Fig. 5 shows that the drain components $C_{\rm dq}$ and $g_{\rm dq}$ of quantum capacitance and quantum transconductance are relatively large, i.e., of the same order as the source components, and that they are nonlinear in a GFET, unlike a conventional MOSFET (where $C_{\rm dq}$ and $g_{\rm dq}$ are essentially zero [25]). Comparing the capacitance-voltage and transconductance-voltage relationships of the source and drain components in Fig. 5, it is evident that the resulting second-order coefficients in (1)–(4), determined by the first derivatives of the curves, would be comparable. On the other hand, the minima in $C_{\rm dq}$ and $g_{\rm dq}$ make the third-order coefficients (determined by the second derivatives) of the drain components much larger than the almost zero third-order coefficients of the source components. The drain components can thus be expected to produce more distortion than the source components in a GFET.

ii) The common-source configuration of the device makes the small-signal gain negative, which means that the small-signal drain voltage v_d is 180° out of phase with the small-signal gate voltage v_g, and hence with the small-signal channel potential $v_{\rm scf}$ (which will tend to follow v_g). This phase difference makes the control voltage $(v_{\rm d} - v_{\rm scf})$ for the drain components of Fig. 3, governed by (2) and (4), bigger than the corresponding control voltage $v_{\rm scf}$ for the source components, governed by (1) and (3). The larger control voltage enhances the distortion coming from the drain components.

The following discussion highlights some of the outcomes of this unique drain dominance in GFET linearity.

1) Effect of Drain Bias on Linearity: One obvious outcome of the drain dominance on GFET linearity is an expected drain-bias dependency of the overall linearity. Fig. 10 shows the IIP3 of the GFET versus gate bias, at a few different values of drain bias.

As can be seen from the figure, in region 1 (constant linearity), a larger drain bias makes the device more linear. This outcome can be explained with the help of Fig. 11, which shows

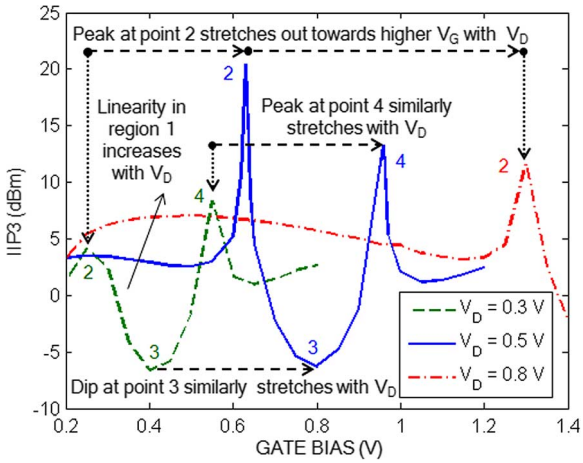

Fig. 10. Simulated IIP3 versus gate bias, at a few different values of drain bias.

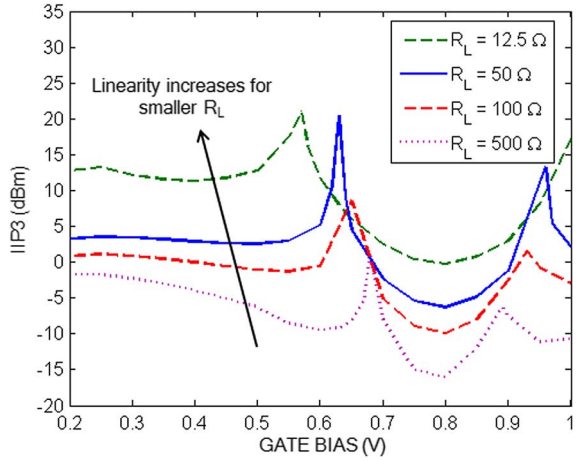

Fig. 12. Effect of load resistance R_L on GFET IIP3 values obtained from simulation.

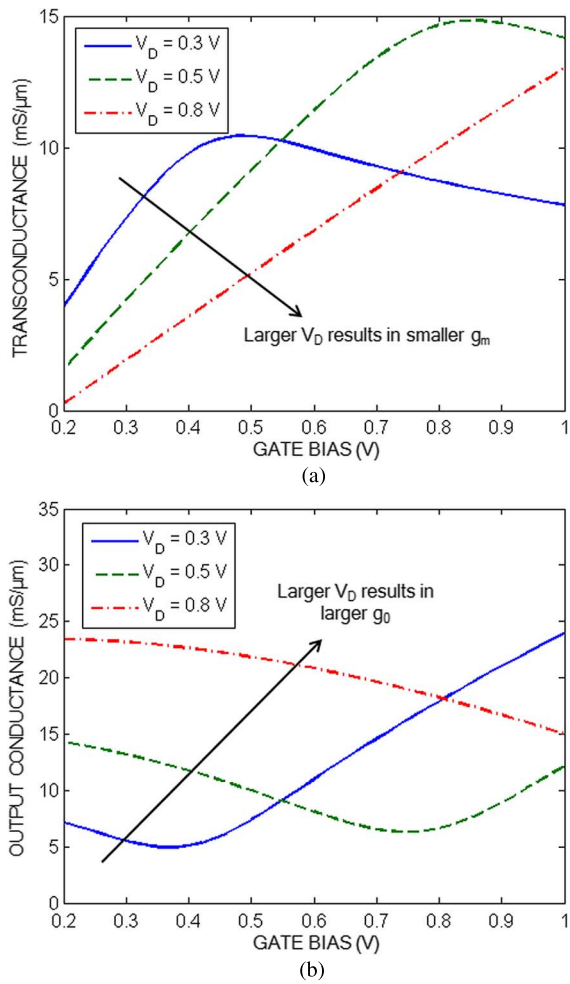

Fig. 11. Simulation results for (a) transconductance and (b) output conductance versus gate bias for varying drain bias.

that in this region, a larger drain bias reduces the transconductance g_m and increases the output conductance g_o. Since the available small-signal voltage gain of the GFET depends on the ratio g_m/g_o, the larger drain bias results in a smaller small-signal voltage gain and, hence, a smaller v_d. A reduced v_d means that the control voltage $(v_d - v_{scf})$ for the drain components is also reduced, which can be expected to reduce the distortion from the drain components in Fig. 3 [according to (2) and (4)] and make the GFET more linear.

A larger drain bias also *stretches* the IIP3 curve, pushing the peaks at points 2 and 4, along with the dip at point 3, toward higher gate biases. The straightforward reason for this outcome is that a larger gate bias is required to push the dc channel potential (Dirac point on a band diagram) down to the lower drain Fermi level at higher drain bias.

2) Effect of Load Resistance on Linearity: Another outcome of the drain dominance on GFET linearity is the effect of the load resistance R_L. A larger R_L results in a larger swing in the drain voltage v_d, which enhances the amount of distortion from the drain components through a larger control voltage $(v_d - v_{scf})$ in (2) and (4). On the other hand, a smaller R_L results in a smaller swing in v_d and the distortion becomes smaller. Fig. 12 shows the effect of R_L on IIP3, while the source resistance is held at 50 Ω. As anticipated, reducing the load from 50 Ω to 12.5 Ω dramatically increases the GFET IIP3 by almost 10 dB. Similarly, increasing the value of R_L degrades linearity.

The unique zero bandgap of graphene (the reason behind the drain dominance) thus makes it possible to improve the linearity, by reducing the load resistance. However, before reducing R_L to improve the linearity, one must consider its implications on the voltage and power gains of the device, two desirable properties of any FET operating at RF frequencies.

a) Voltage gain: The large output conductance of a GFET limits the voltage gain achievable from these devices. For example, Fig. 11 shows that for a drain bias of 0.5 V, the maximum (open-circuit) voltage gain available from the GFET is $g_m/g_o \approx 1.2$ V/V at a gate bias of 0.5 V. The voltage gain becomes even smaller when the device is loaded with a finite R_L. Table I shows that the small R_L of 12.5 Ω that makes the GFET very linear in Fig. 12 also reduces the voltage gain to a mere 0.1 V/V. An attempt to improve linearity by reducing R_L thus reduces the voltage gain considerably.

b) Power gain: Even though the voltage gain of graphene is poor, a sufficiently wide device can still provide enough power gain (through increased current drive). For example,

TABLE I
EFFECT OF CHANNEL WIDTH AND LOAD IMPEDANCE ON LINEARITY AND GAIN @ 24 GHZ AND 0.5 V OF GATE AND DRAIN BIAS

Channel Width (μm)	R_L (Ω)	$g_o R_L$	IIP3 (dBm)	Voltage Gain (V/V)	Power Gain (dB)
1	12.5	0.125	12.78	0.1	-7.65
	50	0.5	2.59	0.3	-4.21
	100	1	-1.08	0.46	-3.77
10	1.25	0.125	12.78	0.1	2.35
	5	0.5	2.6	0.31	5.78
	10	1	-1.08	0.46	6.23

TABLE II
INTRINSIC AND EXTRINSIC CIRCUIT COMPONENTS OF THE GFET

Intrinsic Components	C_{ge} [aF]	1040
	C_{de} [aF]	233
	C_{se} [aF]	96
	C_{sq1} [aF]	784
	C_{dq1} [aF]	188
	g_{sq1} [mS]	27.74
	g_{dq1} [mS]	6.65
Extrinsic Components	$C_{gd,ext}$ [aF]	40
	$C_{gs,ext}$ [aF]	40
	$C_{sd,ext}$ [aF]	24
	$R_{g,eff}$ [Ω]	220/3
	R_s, R_d [Ω]	50

Table I shows that the 1-μm wide device has a power gain of -3.77 dB with a resistively matched load of 100 Ω, but a 10-μm wide device has a power gain of 6.23 dB with a resistively matched load of 10 Ω, where the degree of matching is indicated by the product $g_o R_L$. The gain of the device can thus be increased by making the device wider and setting $g_o R_L = 1$. For simplicity, here we are discussing the power gain simply as $P_G = P_L/P_{av,s}$, where P_L is the power delivered to the load and $P_{av,s}$ is the power available from the source, under the condition of purely resistive terminations for which we have been examining the IIP3; substantially more gain is available, as indicated, for example, by the maximum available gain (MAG), which is ~30 dB for the 1-μm device [7].

Our conclusions on the behavior of IIP3 are unaffected by device width (Table I), as long as we compare IIP3 values for the same $g_o R_L$. Hence, we can now consider a wider device, providing more power gain, and consider again the tradeoff between load resistance and linearity. For example, for the 10-μm wide device, reducing the load from 10 Ω to 1.25 Ω will improve the IIP3 from -1.08 dBm to 12.78 dBm, but will decrease the power gain from 6.23 dB to 2.35 dB.

While admittedly examined under highly simplified conditions (resistive terminations and for an intrinsic device), the key point from this discussion is that the results in Fig. 12 and Table I demonstrate that a reduction in R_L does have the potential to improve linearity in a GFET, unlike conventional FETs, subject to the caveats of reduced voltage and power gain. We will re-examine this issue when external parasitics are introduced (Section III-D below).

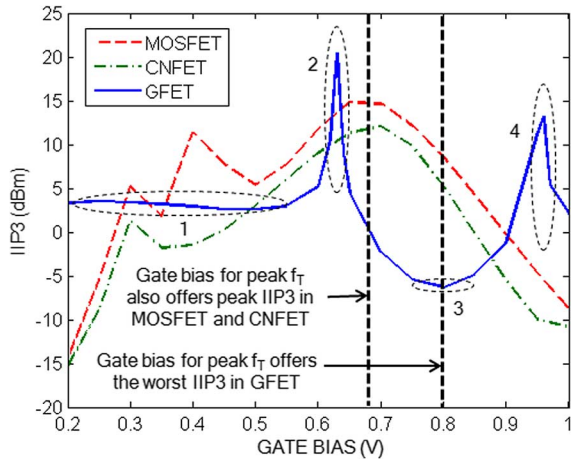

Fig. 13. Simulated intrinsic linearity performance potential comparison of a GFET with its MOSFET and CNFET counterparts. The region 1 and points 2-4 from Fig. 4 for the GFET curve are marked. We have also indicated that the peak IIP3 for a CNFET and MOSFET occur at the same gate bias as peak f_T, whereas for a GFET, the minimum IIP3 occurs at the gate bias for peak f_T. The GFET f_T curve is available in Fig. 4; the MOSFET and CNFET f_T curves are not shown.

C. Linearity of a GFET versus a MOSFET and a CNFET

1) Third-Order Intermodulation Distortion: In order to determine if a GFET holds any promise in RF electronics in terms of linearity, we need to benchmark its performance against its competitors. As a basis for comparison, we simulated the linearity of a silicon MOSFET and an array-based CNFET with identical channel length ($L = 18$ nm), channel width ($W = 1$ μm), and gate capacitance; these are the devices illustrated in [Fig. 1, 25]. The CNFET had 100 tubes (tube pitch = 10 nm) in the channel to obtain a drive current comparable to the other devices. All three devices (including the GFET) were tested with 50-Ω two-tone sources and 50-Ω load terminations and the IIP3 values were recorded against gate bias. For the comparison, we retain the focus on the linearity of the intrinsic transistor so that the emphasis in our comparison is on differences arising from the channel material. Fig. 13 shows that the GFET offers linearity that is, overall, comparable to its MOSFET and CNFET counterparts under this scenario. However, two differences can be flagged. First, as already discussed, the drain dependence of the GFET offers us with an opportunity to enhance its linearity by increasing the drain bias V_D or by lowering R_L, which is not possible in the other devices. Second, the GFET's linearity offers a sweet spot prior to and after peak f_T; these are the points 2 and 4 discussed earlier in conjunction with Fig. 4. In fact, the GFET offers its worst IIP3 at peak f_T, unlike the MOSFET and the CNFET, both of which offer their best IIP3 at peak f_T.

2) Second-Order Distortion: While we have focused on third-order distortion, second-order distortion can also be important in certain RF applications [38]. For example, two out-of-band jammers can mix via a second-order intermodulation product, creating undesired components at the sum and difference frequencies, each of which could land on the fundamental frequency. We will focus on the sum frequency for the sake of this discussion.

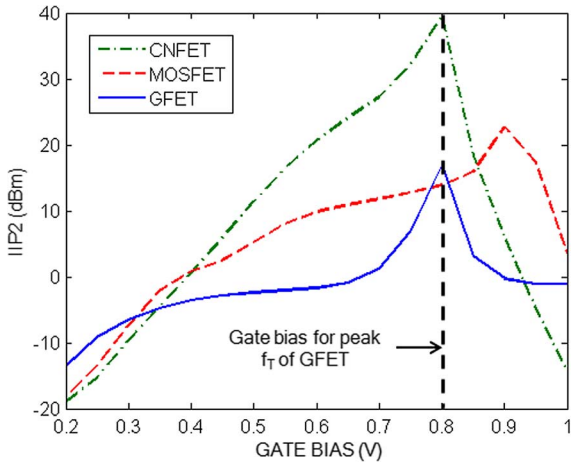

Fig. 14. Simulated intrinsic IIP2 versus gate bias of a GFET compared with its MOSFET and CNFET counterparts.

For the second-order distortion at the mixing frequency $f_1 + f_2$, the GFET suffers from poor linearity when compared to its MOSFET and CNFET counterparts (Fig. 14). This outcome is primarily because of the linear DOS and zero bandgap of graphene, which cause all four quantum capacitances and transconductances of the GFET (source and drain components) to contribute to the distortion.

Fig. 15 shows the relevant quantum capacitances and transconductances for the three devices. Fig. 15(a) shows $C_{\rm sq}$ for all three devices, as well as $C_{\rm dq}$ for the GFET, noting $C_{\rm dq} \approx 0$ for the CNFET and MOSFET; similarly, Fig. 15(b) shows $g_{\rm sq}$ for all three devices, as well as $g_{\rm dq}$ for the GFET, noting $g_{\rm dq} \approx 0$ for the CNFET and MOSFET.

As illustrated in Fig. 15(a), $C_{\rm sq}$ for the CNFET and MOSFET tend to flatten out with bias, which results in small values of the second-order coefficients (determined by the first derivatives of the shown curves) in the Taylor-series expansion (1) for these devices; the coefficients in (2) are zero since $C_{\rm dq} \approx 0$ in a CNFET and MOSFET, due to the existence of a bandgap in the corresponding channel materials. On the other hand, *both* $C_{\rm sq}$ *and* $C_{\rm dq}$ show significant slope over most bias values for the GFET, causing the coefficients in *both* (1) *and* (2) to be pronounced for the GFET.

Similar results follow from inspection of Fig. 15(b), which suggests pronounced distortion from (3) *and* (4) for the GFET, but only (3) for the MOSFET and neither for the CNFET.

Overall, the GFET will hence have second-order distortion contributions from *all four* nonlinear elements in Fig. 3, whereas only one or two of the components will play a role for the CNFET and MOSFET; the GFET thus exhibits the worst IIP2.

One subtle point about the GFET's IIP2 curve should be noted. Unlike the GFET's IIP3, its IIP2 peaks (sharply) at the gate bias for peak f_T. This outcome can be attributed to the minima in the drain components $C_{\rm dq}$ and $g_{\rm dq}$ at that bias point (as shown in Fig. 15 and earlier in Fig. 5), which makes the second-order coefficients determined by the first derivatives very small.

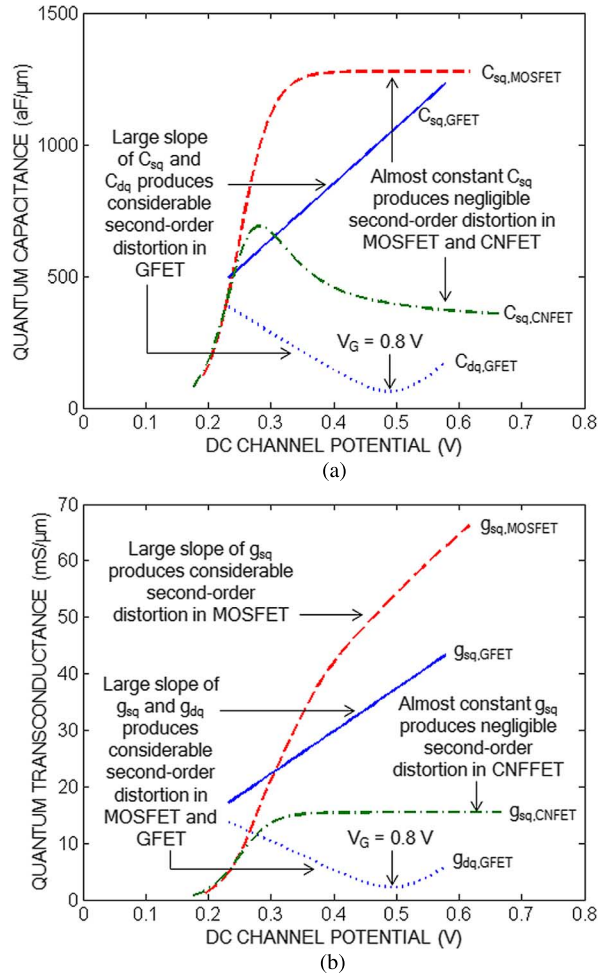

Fig. 15. (a) Relevant quantum capacitances and (b) transconductances versus channel potential for a GFET, MOSFET, and CNFET. The curves are plotted from simulations under an applied gate bias of 0.2 V to 1 V.

D. Extrinsic Linearity of GFET

1) Calculation of Parasitics: To calculate the extrinsic parasitics, the gate contact was assumed to be made of tungsten with dimensions $W \times L_g \times t_g$ of 1 μm × 18 nm × 60 nm. Tungsten was chosen due to its closely matched work-function with graphene. From the resistivity of tungsten, the total resistance of the gate contact was calculated to be 220 Ω. The distributed gate resistance was then modeled as a lumped resistance, $R_{\rm g,eff} = 220/3$ Ω. The source and drain contact resistances were taken to be $R_s = R_d = 50$ Ω, near the theoretical minimum for graphene [39], [40]. The extrinsic capacitances were measured to be $C_{\rm gd,ext} = 40$ aF, $C_{\rm gs,ext} = 40$ aF, and $C_{\rm sd,ext} = 24$ aF by simulating the open-pad structure in COMSOL [32].

Table II lists the intrinsic and extrinsic circuit component values of the 1-μm wide GFET studied in this work; the bias-dependent values were calculated for gate and drain voltages both equal to 0.5 V, and only the first-order coefficients are listed for the nonlinear elements.

2) Extrinsic Linearity Features of a GFET: Once developed, the final extrinsic equivalent circuit was simulated in MWO [33]and the resulting IIP3 values are plotted versus gate bias in

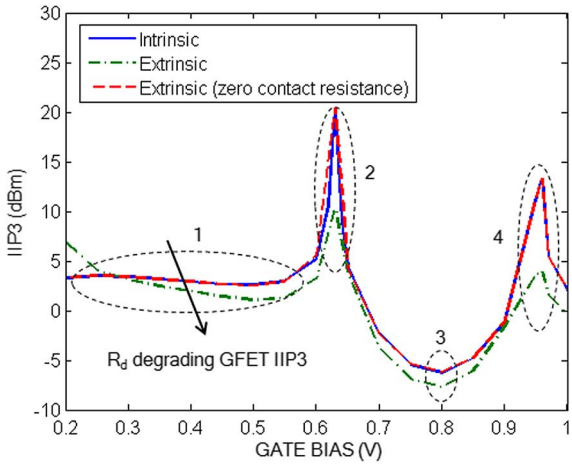

Fig. 16. Simulated intrinsic and extrinsic IIP3 versus gate bias.

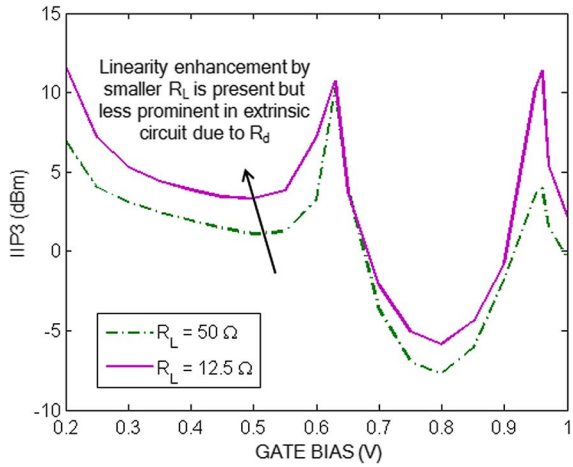

Fig. 17. Effect of load resistance R_L on GFET extrinsic IIP3. The improvement in IIP3 with a reduction in R_L is less pronounced than in the intrinsic case shown in Fig. 12. The IIP3 values were obtained from simulation.

Fig. 16. For the 1-μm wide device, the external parasitics were found to slightly degrade the device linearity, but the signature shape identified from the intrinsic device remains, as demonstrated in Fig. 16.

By selectively removing the parasitics one by one from the circuit in Fig. 3 and solving in MWO, we found that the extrinsic *capacitances* do not affect the RF linearity of GFETs; rather, it is the *contact resistances*. The following discussion identifies the contribution of the contact resistances to GFET linearity.

3) Impact of Drain Contact Resistance: Our investigation showed that the drain contact resistance is primarily responsible for degrading the overall RF linearity of the GFET. The potential drop across the drain contact resistance added to the output voltage $v_{\mathrm{d,ext}}$ results in a larger intrinsic drain voltage v_{d} in the circuit of Fig. 3. As discussed in Section III-B, a larger v_{d} increases the distortion from the nonlinear drain components in Fig. 3, a phenomenon unique to GFETs, and makes the device more nonlinear, by increasing the control voltage $(v_{\mathrm{d}} - v_{\mathrm{scf}})$ in (2) and (4).

It should be mentioned that the source contact resistance will tend to improve the linearity of the device slightly due to its well-known feedback effect in the common-source configuration [41, p. 101], but any such improvement is dominated by the degrading effect of the drain resistance.

The gate contact resistance is small enough in the 1-μm wide device that it does not affect the linearity; we will shortly consider a wider device to isolate its effect.

Simulating the extrinsic circuit with zero R_d while retaining the parasitic capacitances results in identical linearity between the extrinsic and intrinsic devices, as shown in Fig. 16. A small drain resistance is hence essential to making a GFET as linear as possible.

One other note should be made about the impact of the drain resistance. In Section III-B, it was shown that a small R_L has the potential to improve the GFET linearity by reducing the swing of the drain voltage v_d (Fig. 12). However, the presence of the drain contact resistance makes it impossible to lower the swing of v_d enough to improve linearity significantly. Fig. 17 shows the effect of variation in R_L on linearity for the extrinsic GFET. The reduction in R_L that improved the linearity by almost 10 dB in the intrinsic circuit only improves the linearity by 2.2 dB in the extrinsic circuit. Keeping the drain contact resistance low is hence also important to allow for potential linearity improvement by adjusting R_L.

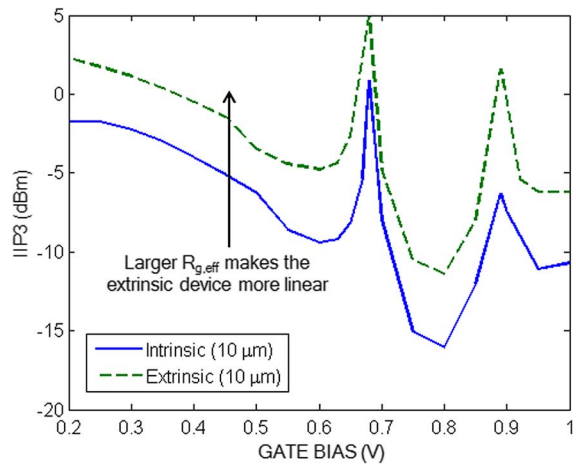

Fig. 18. Simulated intrinsic and extrinsic IIP3 versus gate bias for a 10-μm wide GFET.

4) Effect of Gate Contact Resistance: To examine the impact of $R_{\mathrm{g,eff}}$, a wider device ($W \geq 10$ μm) must be considered, where $R_{\mathrm{g,eff}}$ is appreciable. Fig. 18 shows that the linearity of the 10-μm wide device improves significantly when the effects of the external parasitics are included. The drain contact resistance still degrades the linearity, but the degradation is canceled by an even greater improvement in linearity due to the gate contact resistance $R_{\mathrm{g,eff}}$. As device width increases, the gate contact resistance can hence improve linearity, but this would, of course, come at the expense of reduced power gain.

IV. Qualitative Comparison with Experimental Results

Finally, we compare our IIP3 values with experimental results. As discussed in Section I, most experimental studies have considered the linearity of graphene in RF mixers or circuits [14]–[20]. However, Jenkins *et al.*[21, Fig. 4(a)] measured the

linearity of an individual epitaxially grown n-type GFET in a manner that is consistent with our study. Microscopy images of a similar device are shown in [42]. Note that the fabricated device has a much longer channel than our device, which makes a *direct* comparison with our simulation results impossible. However, a *qualitative* comparison with the reported IIP3 values, as shown in Fig. 19 [parts (a) and (b)], demonstrates that the key signature of the GFET IIP3 (regions 1 to 4), as identified in Section III-A, is present even in a long-channel ($L = 700$ nm) fabricated device. In comparing the predicted and experimental data in parts (a) and (b) of Fig. 19, two points should be borne in mind. First, the *actual* gate bias and IIP3 values should not be expected to overlap, as the two devices involved have different channel lengths; of relevance are the *relative* positions of the identified regions and points with respect to gate bias, and the resulting *signature* in the IIP3 behavior. Second, to assign our identified regions to the experimental plot without ambiguity, we have used points 6 and 3 as *anchors*; point 6 corresponds to the minimum in power gain, and point 3 corresponds to the maximum in power gain. With these two points noted, Fig. 19 shows good overall qualitative agreement between the predicted signature [part (a)] and experimental results [part (b)].

Extending the gate bias values beyond the 0.2 V to 1 V range used throughout our study thus far shows that our approach is capable of capturing most features present in the experimental IIP3 curve [21]. Regions 5, 6, 7, and 8 in the extended plot in Fig. 19(a) clearly mirror the corresponding regions in Fig. 19(b). The mechanism behind these regions can be revealed by examining our developed nonlinear model.

- Regions 5 and 8 are similar to region 1, in which the IIP3 values are relatively insensitive to gate bias. In these regions, we found that the source and drain quantum capacitances and transconductances vary linearly with voltage (consistent with extrapolating the curves in Fig. 5). Therefore, the IIP3 remains almost constant.
- Point 6 occurs at the point of minimum conduction, such that the small-signal transconductance g_m is zero. This zero transconductance results in a small-signal voltage gain A_v of zero. The output of the device therefore contains distortion due to the nonlinear circuit components, but the fundamental frequency component is absent. This makes the device extremely nonlinear at this bias point.
- Point 7 shows another peak in IIP3. By separately examining the nonlinearity of the source and drain components in the small-signal circuit, we found that the contributions to distortion from the source and drain components at point 7 are of equal magnitude and opposite phase. This results in a destructive combination of distortion components, resulting in an IIP3 peak.

However, a few discrepancies do exist.

- Region 1 has a much smaller span in the experiment versus the simulation [Fig. 19(a)], but it should be noted that this region appears between the peaks at 7 and 2, and that its extent depends strongly on the drain bias, as discussed in Section III-B in conjunction with Fig. 10. This drain-bias dependence of the extent of region 1 is confirmed by comparing the simulation results in Figs. 19(a) and 19(c), where a narrower region 1 can be observed in the simulation of Fig. 19(c) [corresponding to $V_D = 0.3$ V] vs. Fig. 19(a) [corresponding to $V_D = 0.5$ V].

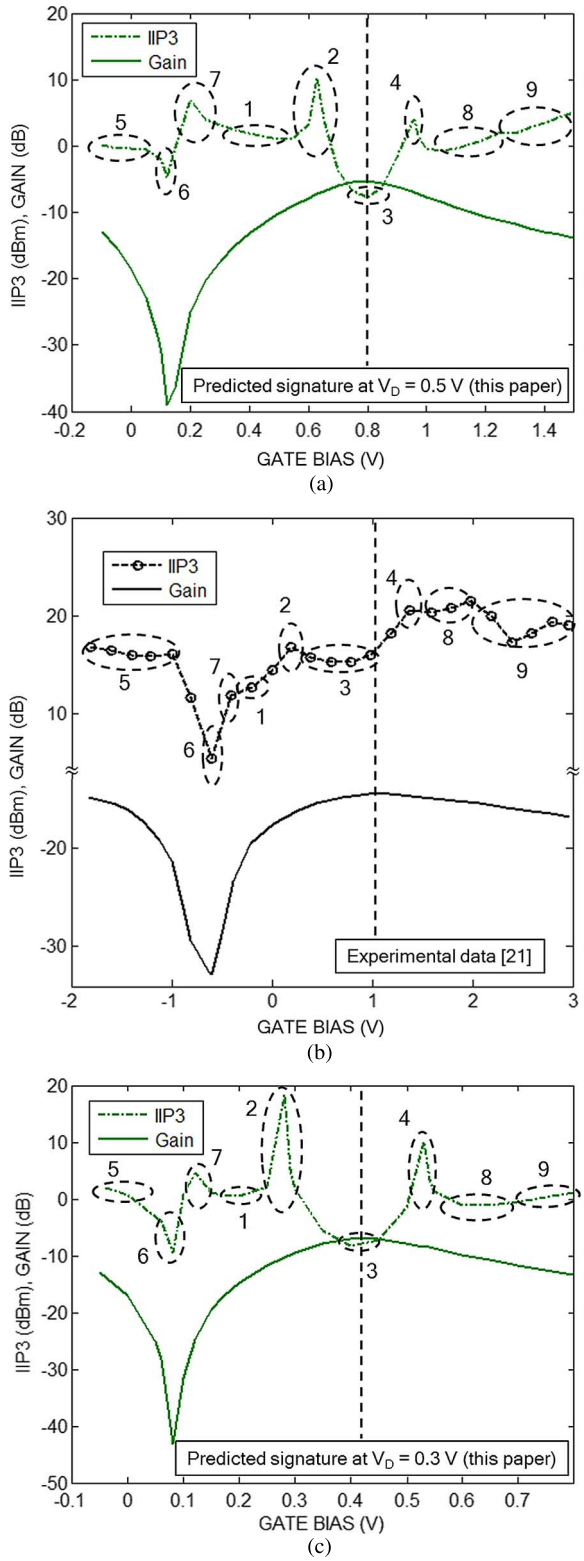

Fig. 19. Qualitative comparison of simulated (extrinsic) IIP3 values of the GFET under investigation in this paper at drain biases of (a) 0.5 V and (c) 0.3 V with (b) experimental data [21, Fig. 4(a)]. We have also shown the power gain in each case for reference.

- fThe peaks at points 2 and 4 are diminished in the experimental IIP3, and the dip around point 3 is also less prominent. The differences between the experimental data and the numerical results are most likely due to the nonidealities in the practical device that our model does not consider, such as scattering. The fabricated GFET in [21] is a long-channel device with a channel length of 700 nm. The transport in this device is therefore subject to scattering, which is neglected in the short-channel GFET ($L = 18$ nm) considered in this study. As discussed in Section III-A, the formation of the peaks at points 2 and 4 is dependent on the phase relationship of the distortion generated by the second- and third-order coefficients of the drain components $C_{\rm dq}$ and $g_{\rm dq}$. The presence of scattering in the long-channel device may change this phase relationship by requiring a modification of the circuit in Fig. 3, which is strictly valid only for ballistic transport, thereby diminishing the peaks.
- Lasy, while both our model and the experiment show a slightly increasing IIP3 moving out toward very high gate bias in region 9, the experimental IIP3 additionally shows a pronounced dip following region 8 that is barely perceptible in the numerical results of Fig. 19(a) and absent in the numerical results of Fig. 19(c). We attribute this difference to a breakdown of our ballistic model in the high bias regime of region 9, as phonon scattering is much more prominent at large gate biases [43], [44].

The similarity of the experimental and theoretical curves in Fig. 19 provides qualitative validation of our modeling approach and resulting observations on the linearity of GFETs. However, this similarity calls for a more detailed investigation and discussion that clarifies why the signature behavior of linearity, which is apparently present at all channel lengths, is governed (for graphene) by features of a ballistic transport model. This investigation and discussion will be pursued separately; here, the most important outcome is that the similarity of experiment and simulations supports our approach and conclusions.

Finally, we observe that the experimental curves shown in Fig. 19(b) show power gain values comparable to our simulation results, but notably higher IIP3 values. Although we should be careful about making quantitative comparisons due to the differences between the two devices, the increased IIP3 in the experimental device suggests that the presence of scattering may *improve* the linearity of GFETs. One reason may be that scattering linearizes the current-voltage behavior. As seen in Fig. 2, the ballistic device in our study shows no saturation in the current-voltage characteristics, whereas experimental devices will likely exhibit stronger saturation due to phonon scattering [45], and therefore better linearity. Confirming this hypothesis would require a careful inclusion of the effects of scattering in our nonlinear model (e.g., via the method outlined in [46]), which is beyond the scope of our present study.

V. Conclusions

The following conclusions can be drawn regarding the RF linearity potential of GFETs.

1) The IIP3 versus gate bias curve of the GFET has four distinct features. A constant linearity region, two sharp peaks, and a large dip.
2) The linear DOS of graphene results in a linear quantum capacitance and transconductance versus voltage relationship in GFETs at low gate bias ($0.2\ \text{V} \leq V_G \leq 0.5\ \text{V}$), which is responsible for the constant linearity region.
3) Depending on the gate bias, the GFET linearity is dictated either by distortion generated by second-order coefficients or by third-order coefficients in the Taylor-series expansions of the nonlinear components. A destructive combination of distortion from the two mechanisms in the transition regions creates sharp peaks in the IIP3 curve.
4) The GFET offers its worst linearity at peak f_T.
5) Over all gate bias values, the distortion generated in the nonlinear drain components dictate the GFET linearity. This is an outcome of the zero bandgap of graphene. It also makes the RF linearity highly sensitive to variations in drain bias and potentially load resistance.
6) In terms of third-order distortion, the GFET's performance is comparable to its MOSFET and CNFET counterparts, with the distinguishing feature that the peak IIP3 does not occur at peak f_T.
7) Due to its linear DOS and lack of a bandgap, the second-order distortion is much worse in a GFET than in its competitors.
8) The extrinsic IIP3 retains the key features (signatures) of the intrinsic IIP3.
9) Parasitic capacitances have a minimal impact on GFET linearity.
10) The drain contact resistance degrades the linearity of a GFET, while the source resistance has minimal impact; this occurs due to the drain dominance of GFET linearity (conclusion 5). In wide devices ($W \geq 10\ \mu$m), the gate contact resistance can make the device more linear but will degrade the power gain.
11) Qualitative agreement between our results and published experimental data [21] supports our approach and conclusions.

Overall, the most important outcomes of this work are the identification of the signature behavior and the drain dependence of graphene linearity. We also showed that graphene has the potential to offer third-order linearity at least comparable to CNFETs and MOSFETs, but suffers from worse second-order linearity. The load-resistance dependency creates a unique opportunity to improve the linearity in GFETs by using smaller loads, but at the cost of reduced voltage and power gain. All these key outcomes are intimately tied to the lack of a bandgap and linear DOS of graphene.

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Ahsan Ul Alam received the Ph.D. degree in electrical engineering from the University of Alberta, Edmonton, AB, Canada, in 2015.

He is currently an Applications Engineer at Lumerical Solutions, Inc., Vancouver, BC, Canada. His research interests include the modeling and simulation of micro- and nanoscale electronic and optoelectronic devices for current and future technologies.

Dr. Alam received the George Walker Award as the top Ph.D. student convocating from the electrical and computer engineering department in the 2015 Spring convocation. He was also nominated for the Governor General's Gold Medal for his accomplishments as a Ph.D. student.

Kyle David Holland received the B.Sc. degree in 2009 in engineering physics (nanoengineering option) from the University of Alberta, Edmonton, AB, Canada, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests are in the quantum simulation of carbon-based nanoelectronics, with an emphasis on modeling the high-frequency performance of graphene devices.

Mr. Holland currently holds an NSERC Alexander Graham Bell Canada Graduate Scholarship and an Alberta Innovates Graduate Student Scholarship, and he was a recipient of the Ralph Steinhauer Award of Distinction.

Michael Wong received the B.Sc. degree in computer engineering in 2013 from the University of Alberta, Edmonton, AB, Canada, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include modeling and simulation of nanoscale devices, including FinFETs and 2D FETs.

Mr. Wong currently holds the Natural Sciences and Engineering Research Council of Canada Alexander Graham Bell Canada Graduate Scholarship and the Alberta Innovates Graduate Student Scholarship. He has also received The Rt. Hon. C. D. Howe Memorial Fellowship at the University of Alberta.

Sabbir Ahmed received the B.Sc. and M.Sc. degrees in electrical and electronic engineering (EEE) from the Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, in 2005 and 2007, respectively and the Ph.D. degree in electrical and computer engineering from the University of Alberta, Edmonton, AB, Canada in 2014.

He is currently an Electrical & Control System Design Engineer with Stantec Consulting Ltd., Calgary, AB, Canada. From 2005 to 2008, he was a Lecturer with the Department of EEE of BUET. His research interests include the theory, modeling, and simulation of nanoscale electronic devices, with an emphasis on the high-frequency and circuit-level performance of III-V high-electron-mobility transistors, carbon-based transistors, and solar-cell devices.

Dr. Ahmed received the F. S. Chia Doctoral Scholarship in 2008 and 2009, and the Queen Elizabeth II Graduate Scholarship in 2010, 2011, and 2012 at the University of Alberta.

Diego Kienle received the B.S. (Vordiplom) and M.S. (Diplom) degree from the University of Bayreuth, and his PhD (Dr.rer.nat.) from the Research Center Jülich and the University of Saarland, Germany, in theoretical physics.

After appointments with the Electrical and Computer Engineering Department at Purdue University and the Material Science Department at Sandia National Laboratories in California, he is currently with the Institute of Theoretical Physics at the University of Bayreuth. His research interests are in the theory, modeling, and simulation of ac quantum electronic transport in nanoscale materials and devices with a focus on the understanding of the quantum dynamic processes in low-dimensional materials and their potential application in solid-state-based terahertz devices. His past research interests are in the theory and modeling of complex fluids by means of Brownian dynamics with a focus on many-body hydrodynamic interaction effects in diluted polymer solutions.

Mani Vaidyanathan (S'95–M'99) received the Ph.D. degree in electrical engineering from the University of British Columbia, Vancouver, BC, Canada.

He is currently an Associate Professor with the Department of Electrical and Computer Engineering at the University of Alberta, Edmonton, AB, Canada. His research interests include the modeling, simulation, and understanding of electronic devices for future electronics, with a present focus on the radio-frequency performance of FinFETs and 2D materials.

Dr. Vaidyanathan is a recipient of the University of Alberta's Provost's Award and the University of Alberta's Alexander Rutherford Award for excellence in teaching.