Switching-Speed Limitations of Ferroelectric Negative-Capacitance FETs

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***Abstract*— Recently, negative-capacitance FETs (NCFETs) have been proposed to reduce subthreshold slope and help continue supply-voltage scaling alongside channel-length scaling. We investigate the high-frequency switching behavior of NCFETs using the Landau–Khalatnikov equation to model ferroelectric materials. Multidomain interactions in the ferroelectric are considered, resulting in strong agreement with experimental measurements. Operation of NCFETs at gigahertz frequencies is investigated with this experimentally validated multidomain model. We find that the effectiveness of the voltage amplification in NCFETs is strongly dependent on the viscosity coefficient ρ of the ferroelectric, and that a low ρ ($<0.1\ \Omega \cdot m$) is required for the operation at the high gigahertz frequencies.**

***Index Terms*— Ferroelectric, Moore's law, negative capacitance, negative-capacitance FETs (NCFETs), subthreshold slope.**

I. Introduction

As MOORE'S law continues and transistors scale to ever-smaller dimensions, the electronics industry is becoming increasingly concerned with managing the power density in large digital chips [1], [2]. One way to reduce this power density is to use transistors with a steep slope, i.e., a low subthreshold swing (SS). However, conventional transistors are fundamentally limited to SS $\geq$ 60 mV/decade by Boltzmann mechanics. Recently, the exploitation of ferroelectric materials has gained much attention as a potential way to break this 60 mV/decade limit [3]–[6].

In ferroelectric materials, the crystal lattice is stable at a state that exhibits a spontaneous polarization, which can be flipped by applying an electric field to deform the crystal to the opposite state [7], [8]. A capacitor made with such a ferroelectric material can exhibit "negative capacitance," where the stored charge in a stable state is negative with respect to the applied voltage. Such negative capacitance can be exploited for "voltage amplification," by making the voltage across a second capacitor placed in series with a ferroelectric larger than that applied to the series combination. This voltage amplification can be exploited in the gate-stack of a transistor in order to achieve SS $<$ 60 mV/decade [3].

Although negative-capacitance phenomena have been studied in various forms [9]–[15], the idea to use ferroelectrics to create "negative-capacitance FETs" (NCFETs), in which voltage amplification from negative capacitance is utilized to realize SS $<$ 60 mV/decade, came to prominence only very recently, as a result of the work of Salahuddin and Datta [3]. Subsequently, negative capacitance in lead zirconium titanate (PZT) was experimentally validated [16], and soon thereafter, NCFETs using ferroelectrics were demonstrated experimentally [17]–[19], with SS values of 42 mV/decade [17] and 8.5 mV/decade [18]. However, all the experimental works done thus far on NCFETs have considered only static (dc) device behavior, rather than dynamic (transient switching) behavior. While a few studies have experimentally measured the transient response of *isolated* ferroelectric capacitors [16], [20], the dynamic response of NCFETs incorporating ferroelectrics thus remains relatively unexplored, especially for operation at frequencies relevant in present-day, high-speed digital electronics.

In this paper, we present a multidomain simulation methodology based on the Landau–Khalatnikov (LK) equation to probe the dynamic behavior of NCFETs. With the parameters of the ferroelectric material calibrated to the experimental data presented in [16], we simulate a digital inverter–inverter configuration and show that, given the ferroelectric materials currently known, NCFETs may lose their advantage over conventional FETs when operating at frequencies in the gigahertz range.

II. Methodology

A. Simulated Circuits

We perform two switching simulations in order to investigate the ferroelectric described in Section II-B. The first setup, shown in Fig. 1, emulates the experimental measurement in [16]. An input voltage source v_{IN} stepping

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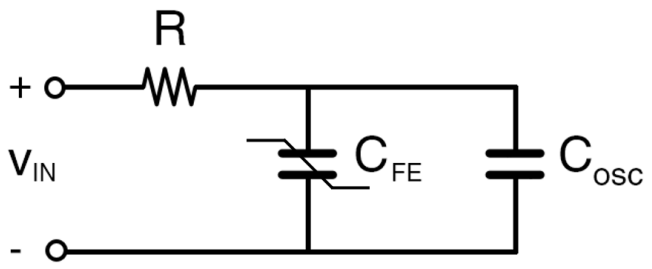

Fig. 1. First simulation setup, corresponding to the experimental measurement in [16].

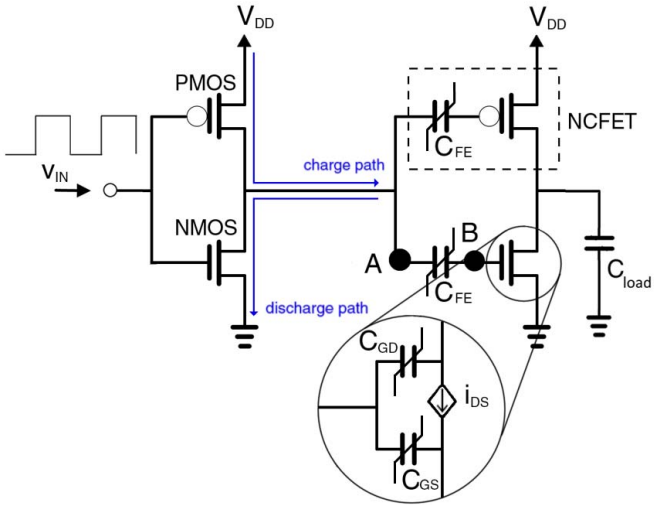

Fig. 2. Second simulation setup, corresponding to a high-speed digital inverter–inverter model.

between −5.4 and +5.4 V, with a period of 120 μs, is placed in series with a 50 kΩ resistor and a ferroelectric (thickness $t_{FE} = 60$ nm and area $A = 30\ \mu\text{m} \times 30\ \mu\text{m}$). An oscilloscope, represented as a 60-pF capacitor C_{OSC}, appears in parallel with the ferroelectric capacitor C_{FE}.

The second setup, shown in Fig. 2, is constructed to obtain an understanding of the impact of ferroelectrics in high-speed digital circuits. We model a digital inverter–inverter configuration at the 28-nm node, with each MOSFET enhanced by a ferroelectric capacitor in series with its gate, the combination thus yielding an NCFET, as shown in Fig. 2. Here, the ferroelectric capacitor has dimensions $t_{FE} = 6$ nm and $A = 90$ nm^2, with the thickness and area chosen for capacitance matching with the MOSFET in order to maximize voltage amplification [3], [21]. The conventional nMOS and pMOS transistors are modeled as voltage-dependent gate capacitances $C_{GS}(v_{GS}, v_{DS})$ and $C_{GD}(v_{GS}, v_{DS})$, combined with a voltage-dependent current source $i_{DS}(v_{GS}, v_{DS})$, where $v_{GS}(t)$ and $v_{DS}(t)$ are the gate–source and drain–source voltages, respectively, both dependent on time t. The voltage dependencies, shown in Fig. 3, were determined using Cadence Spectre simulations [22]. Both nMOS devices have gate dimensions of 30 nm × 30 nm. The pMOS devices have double the channel width as the nMOS devices, with dimensions of 60 nm × 30 nm, in order to reach a similar ON current as the nMOS devices of approximately 20 μA. The supply voltage V_{DD} is taken to be 1 V. We consider the transient behavior of this inverter pair at frequencies varying from 5 to 500 MHz. In the first half of the cycle, the input to the second stage charges to V_{DD} through the pMOS of the first inverter, while in the second half of the cycle, it discharges to ground through the nMOS of the first inverter. In both cases, we use the voltage-dependent current and capacitance data obtained from Cadence Spectre [22], shown in Fig. 3, to determine the circuit response through numerical simulation.

B. Modeling the Ferroelectric

Our simulation methodology is based on the LK equation [23], [24] for a ferroelectric capacitor (C_{FE} in Figs. 1 and 2)

$$\rho \frac{dP(t)}{dt} + \frac{dG}{dP} = 0 \tag{1}$$

where $P(t)$ is the polarization, G is Gibb's free energy, and ρ is the viscosity.

The viscosity ρ in (1) accounts for the resistance of the ferroelectric to deformation, which is the mechanism for polarization switching, and hence, ρ accounts for the finite time required for switching to occur. The expression for Gibb's free energy appearing in (1) is

$$G = \alpha P^2(t) + \beta P^4(t) + \gamma P^6(t) - E(t)P(t) \tag{2}$$

where α, β, and γ are material coefficients specific to a chosen ferroelectric [25], and where

$$E(t) = \frac{v_{FE}(t)}{t_{FE}} \tag{3}$$

is the electric field across the ferroelectric, with $v_{FE}(t)$ being the voltage across it.

Equations (1)–(3) apply to a ferroelectric crystal with a uniform polarization; in order to capture the effect of multiple domains and the resulting nonuniform polarization, we discretize the ferroelectric into a square lattice and consider the area A_i centered around each lattice point i to have a uniform polarization $P_i(t)$. A linear interaction factor ties together all neighboring lattice points [26], [27]. We thus modify (1) and (2) to apply to a nonuniform polarization, finally obtaining

$$\rho \frac{dP_i(t)}{dt} = \frac{v_{FE}(t)}{t_{FE}} + k\left[\sum_j (P_j(t) - P_i(t))\right] - 2\alpha_i P_i(t) - 4\beta_i P_i^3(t) - 6\gamma_i P_i^5(t) \tag{4}$$

where k is the interaction factor that describes the strength of the coupling between the nearest neighbor lattice points, the sum over j is the sum over all neighbors of i, and we assume that the entire ferroelectric crystal experiences a uniform electric field specified by (3). Finally, the charge on the ferroelectric capacitor is given by

$$Q(t) = \sum_i \left[\varepsilon_0 \frac{v_{FE}(t)}{t_{FE}} + P_i(t)\right] A_i. \tag{5}$$

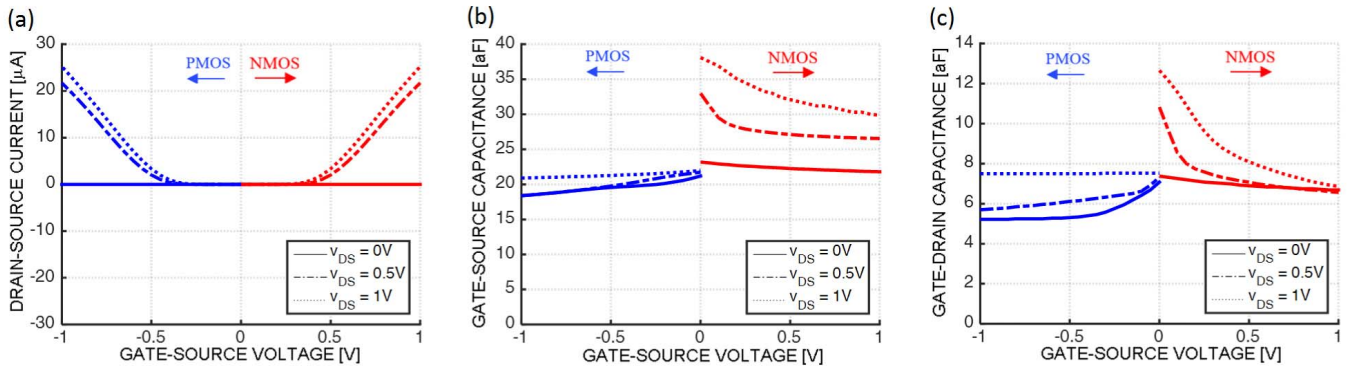

Fig. 3. Cadence Spectre [22] simulation results for a 28-nm FET. (a) $i_{DS}(v_{GS}, v_{DS})$ curves of nMOS and pMOS. (b) $C_{GS}(v_{GS}, v_{DS})$ curves for nMOS and pMOS. (c) $C_{GD}(v_{GS}, v_{DS})$ curves for nMOS (red online) and pMOS (blue online).

Under these assumptions, (4) and (5) specify the nonlinear, time-dependent, charge-voltage (Q–v_{FE}) relation for each element C_{FE}, and they can be used with the corresponding current $dQ(t)/dt$ through each element, and Kirchoff's laws, to determine the transient responses of the circuits in Figs. 1 and 2. The time-domain integration is performed using Euler's method with adaptive time step.

C. Device Parameters

For the ferroelectric, we consider $PbZr_{1-x}Ti_xO_3$, where $x = 0.8$ for the overall crystal. However, in order to capture variations within the ferroelectric, we assume that the material exhibits a random spread, with x uniformly distributed between 0.6 and 1; the resulting coefficients α_i, β_i, and γ_i in (4) can then be obtained using the expressions found in [25]. ρ is fitted at 2 $\Omega \cdot$ m to produce good agreement with the experimental result. The validity of our model and the underlying assumptions are verified by strong agreement with experiment, as shown in Section III-A.

III. Results and Discussion

A. Calibration with Experiment

As shown in the exploded view of Fig. 4, our simulated transient response aligns very well with the experimental curves in [16], including the sharp peak followed by a rapid decay and subsequent rise.

Note that this signature behavior, and particularly the peaking, cannot be properly captured by a simulation that assumes uniform polarization, i.e., a single domain [16, Fig. 4(b)]. A multidomain model [specified by our (4) and (5)] is needed to account for nonuniform polarization. We found that, for the purposes of this calibration to experiment, a square lattice with 100 points in each direction was adequate for reproducing the experimental curves. As the voltage across the ferroelectric v_{FE} climbs, it reaches the threshold required to cause the polarization at one lattice point of the ferroelectric crystal to flip, which, in turn, causes a cascading effect: the flipped polarization at one lattice point spreads to neighboring lattice points via the interaction factor k (modeling the shifting of domain walls), which results in a sharp drop in the electric field, and hence v_{FE}. This drop then slows as the region of flipped domains spreads to cover a greater proportion of the crystal, and v_{FE} resumes its steady climb, driven by the input signal, and the electric field thereby rises sufficiently to help flip the lattice points most resistant to a change in polarization. Clearly, capturing such behavior requires a nonuniform (multidomain) polarization approach.

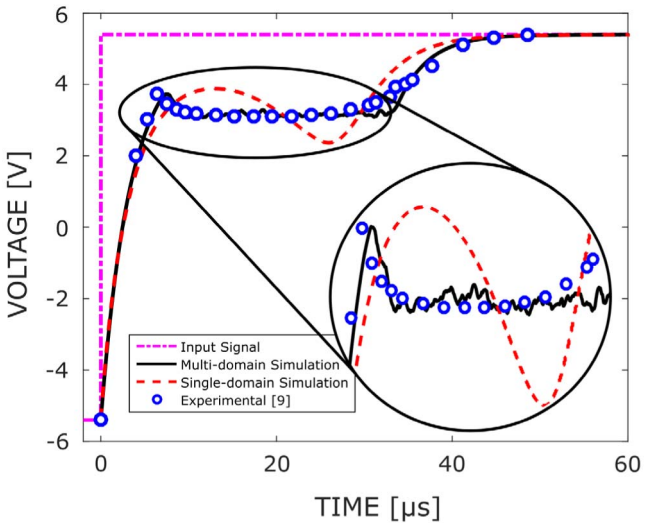

Fig. 4. Validation of our simulation methodology via a comparison with the experimental curves in [16]. Circles show experimentally measured values for the voltage v_{FE} across the ferroelectric. Solid line shows the result of our multidomain simulation, which exhibits a strong match to experiment. Dashed lines show the result of a single-domain simulation. The input voltage is also shown as a dashed-dotted line.

B. Dynamic Behavior at Low Frequencies

Having calibrated our simulation to experiment, we now examine the switching behavior of an inverter (Fig. 2) in order to assess the viability of digital circuits using PZT NCFETs. We first consider operation at a frequency of 5 MHz. As shown in Fig. 5, our simulation confirms the voltage amplification effect of the ferroelectric at 5 MHz. The voltage at the internal node B (Fig. 2) (between the ferroelectric capacitor and the gate of the MOSFET) is 1.4 times greater

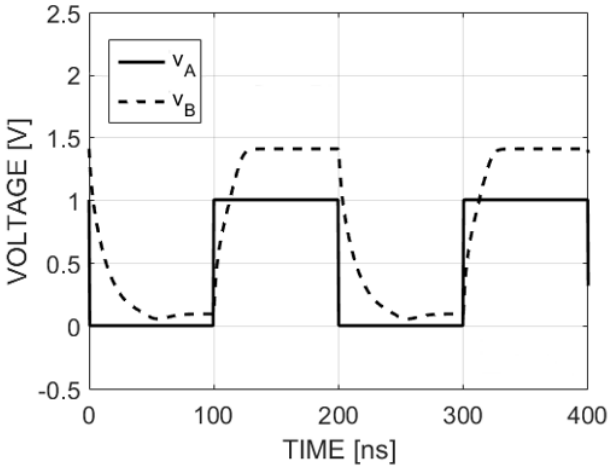

Fig. 5. Dynamic simulation of the circuit of Fig. 2 with an input signal at 5 MHz, showing verification of the voltage amplification effect.

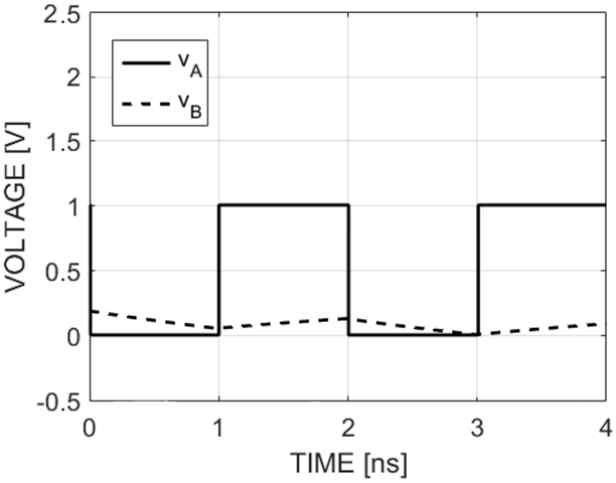

Fig. 6. Dynamic simulation of the circuit of Fig. 2, with an input signal at 500 MHz, showing loss of voltage amplification, i.e., showing $v_B < v_A$, at a higher frequency (versus that for Fig. 5).

than that of node A (to the left of the ferroelectric capacitor), which demonstrates a voltage boosting effect created by the ferroelectric capacitor. This boost will allow for an effective SS lower than 60 mV/decade [3].

C. Dynamic Behavior at High Frequencies

We then consider operation of this circuit at a frequency of 500 MHz. As shown in Fig. 6, at this frequency, the voltage amplification is lost, and the voltage at the internal node B in Fig. 2, i.e., between the ferroelectric capacitor and the gate of the MOSFET, is always lower than the voltage at node A to the left of the ferroelectric. We will now examine the reason for this result.

D. Connection to P–E Hysteresis Curves

The reason for a lack of negative capacitance and hence voltage amplification at high frequencies (Fig. 6) can be understood by considering the P–E hysteresis curves of a ferroelectric. Since the ferroelectric crystal must physically distort in order to switch polarization states, there is a small but finite delay between a voltage input and the resulting response in polarization—a delay modeled through the viscosity ρ in our LK approach. It then follows that for an input at high frequencies, the polarization cannot keep pace, and therefore remains in a fixed state. This gives rise to a *symmetry breaking* effect at high frequencies [28], [29], as shown in the simulated P–E hysteresis curves in Fig. 7, where for illustration, we take E to be the electric field across a single-domain ferroelectric. For frequencies up to 1 GHz, the ferroelectric is able to reach both the positive and the negative polarization. However, as the frequency increases further, and certainly by 10 GHz, the electric field changes too quickly for the ferroelectric to respond, and the polarization remains trapped in one of the two stable states. Due to this trapped polarization state, the ferroelectric capacitor cannot exhibit negative capacitance, and hence voltage amplification cannot occur. These results are consistent with the experimental data for the switching kinetics of PZT; measured rise times are approximately 200 ps [20], suggesting an operating-frequency limit of about 2.5 GHz.

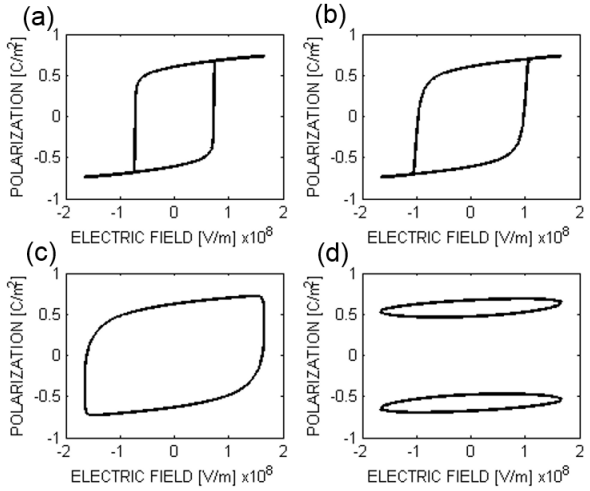

Fig. 7. Hysteresis curves at frequencies of (a) 10 MHz, (b) 100 MHz, (c) 1 GHz, and (d) 10 GHz, showing the symmetry breaking phenomenon at high frequencies.

E. Frequency Effects on Voltage Amplification

The impact of symmetry breaking at high frequencies is shown explicitly in Fig. 8. As shown, the voltage amplification, defined as the peak voltage at node B divided by the peak voltage at node A in Fig. 2, steadily decreases as the frequency increases and as symmetry breaking inhibits polarization switching and the negative-capacitance effect. It is worth adding that at very high frequencies, the insertion of the ferroelectric can actually lead to an attenuation of the voltage at B with respect to A. This phenomenon can be understood by considering the physical implications of the symmetry breaking of ferroelectric materials. At high frequencies, once symmetry breaking occurs [Fig. 7(d)], the ferroelectric is trapped in one of two polarization loops. In this case, the magnitude of the polarization change is small, i.e., the

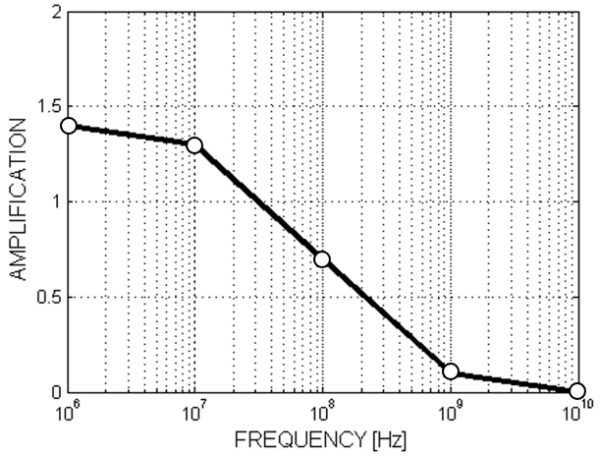

Fig. 8. Dependence of voltage amplification in the circuit of Fig. 2 on frequency, as described in the text.

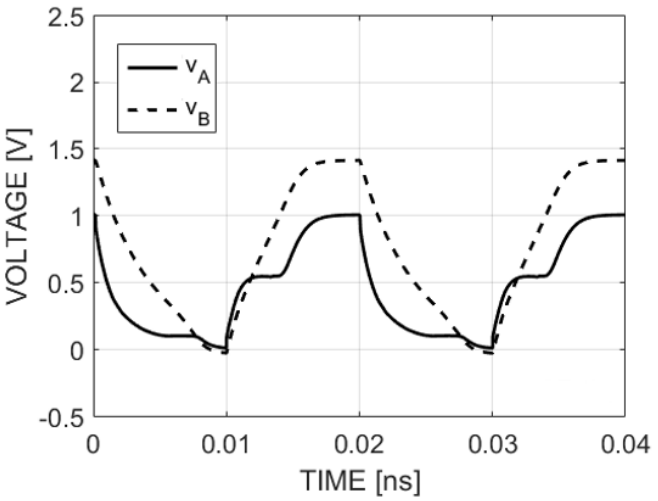

Fig. 9. Dynamic simulation showing voltage amplification in the circuit of Fig. 2 at 50 GHz for $\rho = 0.1$ m$\Omega \cdot$ m.

contribution of the term involving $P_i(t)$ in (5) to the dynamic response is negligible at high frequencies; the ferroelectric behaves essentially as a linear capacitance $\sim \varepsilon_0 A/t_{\rm FE}$ that is small compared with the gate oxide capacitance $\varepsilon_{\rm ox}\varepsilon_0 A/t_{\rm ox}$ of the MOSFET, where $\varepsilon_{\rm ox}$ is the relative permittivity of the oxide and $t_{\rm ox}$ is its thickness, leading to the voltage *attenuation* visible in Fig. 8 at high frequencies.

F. Generalization to Other Ferroelectric Materials

The previous analysis was performed on a specific composition of PZT and there is no obvious extension to other ferroelectric materials. However, with an *RC* circuit approximation of a switching NCFET, we show in the Appendix that the minimum possible time required to achieve voltage amplification within an NCFET configuration is

$$\tau_{\rm min} = \frac{\rho t_{\rm FE}}{2}\left(\frac{C_{\rm MOS}}{A}\right) \tag{6}$$

where $C_{\rm MOS}/A$ is the usual capacitance per unit area of the gate.

With this expression, we can determine a bound for ρ to obtain $\tau_{\rm min} = 1$ ps, where 1 ps corresponds to the rise time of the inverter–inverter circuit in Fig. 2 in the absence of a ferroelectric material, i.e., the rise time with usual MOSFETs as opposed to NCFETs, and hence, the rise time representative of the modern and future processors working in the gigahertz to terahertz range.

A lower bound on the thickness for ferroelectrics is $t_{\rm FE} = 1$ nm, a value that can be found by accounting for the typical dimensions of a unit cell in ferroelectrics [30], and a reasonable minimum per-unit-area capacitance value for modern MOSFETs is $C_{\rm MOS}/A \sim 30$ fF/μm^2, which can be deduced from the Cadence Spectre [22] simulation results shown in Fig. 3. With these values, to obtain $\tau_{\rm min} = 1$ ps, we find from (6) that ρ must be less than about 0.1 $\Omega \cdot$ m, independent of other material properties, a value considerably lower than the $\rho = 2\ \Omega \cdot$ m value we used to match the experiments for PZT in Fig. 4. In fact, for PZT, using the same α, β, and γ material coefficients as we did for Fig. 4, we find ρ must be reduced to 0.1 m$\Omega \cdot$m to achieve voltage amplification with a 1-ps rise time, as shown in Fig. 9. Note that the required ρ of 0.1 m$\Omega \cdot$m is actually 1000 times lower than the value of 0.1 $\Omega \cdot$m we found from (6), emphasizing that the latter value represents an *upper bound* on ρ, i.e., a *necessary* condition for any ferroelectric material to provide voltage amplification under high-speed operation.

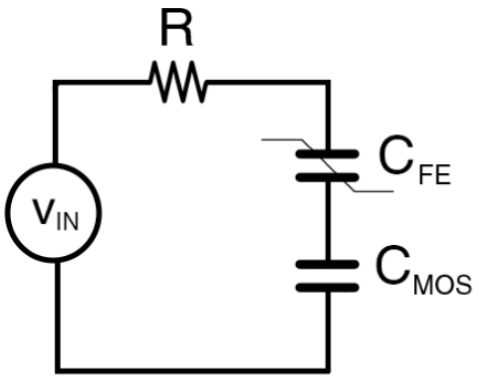

Fig. 10. Simplified NCFET switching circuit, with a voltage $v_{\rm IN}$ applied to the gate.

IV. Conclusion

The following conclusions can be drawn from this paper examining NCFETs operating under high-speed switching conditions.

1) Current studies on NCFETs focus on static measurements of subthreshold slope. We have identified an additional parameter ρ that strongly influences the high-frequency response of ferroelectric materials.
2) The transient switching simulation results presented in this paper show that while ferroelectrics do have the potential to provide voltage amplification, and hence an enhanced response to gate voltages in the megahertz range, they will cease to provide this advantage in the gigahertz to terahertz range.

3) Ferroelectric materials must have a viscosity coefficient ρ less than 0.1 $\Omega \cdot$ m to achieve voltage amplification with a 1-ps rise time.

While the requirement for a very low ρ may make NCFETs unsuitable for high-speed processors, they may still find application in low-speed applications, such as low-power sensors or low-power embedded systems, where polarization switching, negative capacitance, and voltage amplification will still occur. For high-speed applications, work is required to find a material with a suitably low ρ (below 0.1 $\Omega \cdot$ m).

APPENDIX

We derive a minimum switching time for a ferroelectric capacitor regardless of the ferroelectric material used. For this analysis, as shown in Fig. 10, we consider a simplified circuit consisting of a voltage source v_{IN}, resistor R, ferroelectric capacitor C_{FE}, and linear capacitor C_{MOS} in a series circuit, representing the relevant properties of a switching NCFET.

We can say that the negative capacitance of the ferroelectric capacitor has provided a benefit if the voltage across the linear capacitor is greater than the voltage of the source. For simplicity, we use the single-domain LK equation

$$\rho \frac{dP(t)}{dt} = E_{\mathrm{ext}}(t) - 2\alpha P(t) - 4\beta P^3(t) - 6\gamma P^5(t) \quad (7)$$

and consolidate the polarization polynomial into a single variable $E_{\mathrm{int}}(t)$ with units of V/m

$$\rho \frac{dP(t)}{dt} = E_{\mathrm{ext}}(t) - E_{\mathrm{int}}(t) \quad (8)$$

where $E_{\mathrm{ext}}(t)$ is the applied electric field across the ferroelectric capacitor and $E_{\mathrm{int}}(t) = 2\alpha P(t) + 4\beta P^3(t) + 6\gamma P^5(t)$.

We now consider a single switching cycle, with v_{IN} increasing from 0 to a constant voltage $V_S > 0$, which eventually causes the ferroelectric capacitor to flip, and hence an amplified voltage to appear across the linear capacitor. During this process, we know that the maximum applied electric field must be below V_S/t_{FE}, i.e., $E_{\mathrm{ext}}(t) \leq V_S/t_{\mathrm{FE}}$ for all t, because the ferroelectric capacitor cannot have more voltage across it than the source supplies. We assume that the maximum magnitude of the internal field remains below the coercive electric field E_C [31], i.e., the field required to flip the polarization; hence, $|E_{\mathrm{int}}(t)| \leq E_C$, which is a necessary condition for the ferroelectric to provide voltage amplification [3]. The coercive electric field E_C must also be lower in magnitude than V_S/t_{FE}, because we have assumed that V_S is large enough to flip the ferroelectric capacitor. Therefore, the maximum magnitude of the internal field is also below V_S/t_{FE}, i.e., $|E_{\mathrm{int}}(t)| \leq V_S/t_{\mathrm{FE}}$. Thus, we can derive a maximum value for $E_{\mathrm{ext}}(t) - E_{\mathrm{int}}(t)$ of $2V_S/t_{\mathrm{FE}}$ in the presumed switching cycle, occurring when a maximum $E_{\mathrm{ext}}(t) = V_S/t_{\mathrm{FE}}$ is applied to flip the ferroelectric while $E_{\mathrm{int}}(t) = -V_S/t_{\mathrm{FE}}$ retains its maximum magnitude but is opposite in sign

$$\rho \left.\frac{dP(t)}{dt}\right|_{\max} = [E_{\mathrm{ext}}(t) - E_{\mathrm{int}}(t)]_{\max} = 2\frac{V_S}{t_{\mathrm{FE}}}. \quad (9)$$

We can also make an approximation on the charge accumulated on the ferroelectric capacitor

$$Q(t) = \int \left[\varepsilon_0 \frac{v_{\mathrm{FE}}(t)}{t_{\mathrm{FE}}} + P(t)\right] dA \approx P(t)A \quad (10)$$

since for negative-capacitance operation, polarization must dominate the total charge contribution.

From the bounding values specified by (9) and (10), we can find the maximum current flowing through the circuit at any time

$$I_{\max} = \frac{dQ(t)}{dt}|_{\max} = A\frac{dP(t)}{dt}|_{\max} = \frac{2AV_S}{\rho t_{\mathrm{FE}}}. \quad (11)$$

If we determine how long it takes for a constant current of this magnitude to charge up the linear capacitor to a voltage of V_S, we will find the minimum time required for the ferroelectric capacitor to provide voltage amplification

$$\tau_{\min} = \frac{CV_S}{I_{\max}} = \frac{\rho t_{\mathrm{FE}}}{2}\left(\frac{C_{\mathrm{MOS}}}{A}\right). \quad (12)$$

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