RF Performance Limits and Operating Physics Arising From the Lack of a Bandgap in Graphene Transistors

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***Abstract*—With the aid of self-consistent quantum-mechanical simulations and simple expressions for the radio-frequency (RF) metrics, we examine the impact of a lack of a bandgap on limiting the RF potential of graphene transistors. We consider the transconductance, gate-input capacitance, output conductance, unity-current-gain frequency, and unity-power-gain frequency. We show that the lack of a bandgap leads to all RF metrics being optimal when the bias point is chosen such that the drain Fermi level aligns with the Dirac point at the midpoint of the channel. We are also able to quantify the precise extent to which the lack of a bandgap limits the transistor's cutoff frequencies, an issue that has been flagged as requiring crucial attention to make graphene transistors competitive. For an 18-nm channel length, we show that the extrinsic unity-current-gain frequency could be improved by 300 GHz and the unity-power-gain frequency could be doubled if a bandgap could be introduced to reduce the output conductance to zero.**

***Index Terms*—Bandgap, cutoff frequency, field-effect transistor (FET), graphene, high-frequency behavior, output conductance, parasitic capacitance, parasitic resistance, radio-frequency (RF) behavior.**

I. Introduction

SINCE first being used for a field-effect transistor (FET) in 2004 [1], graphene has recently gained great attention as a possible channel material for high-frequency[1] devices. The advancement of graphene transistor technology has been rapid, with the time from initial studies to a functioning GHz-speed radio-frequency (RF) transistor being nearly three times as fast as with carbon nanotubes (CNs) [2]. Currently, the fastest graphene FET (GFET) has a projected intrinsic f_T of 1.4 THz [3], compared with a record of 153 GHz for an array-based carbon-nanotube FET (CNFET) [4].

While several issues still exist in the fabrication of GFETs—such as the creation of high-quality monolayer transistors over a large area [5] and the reduction of access resistance between the channel (under the gate) and the source and drain contacts [3]—a feature unique to GFETs is the lack of an electronic bandgap [6], [7]. The lack of a bandgap leads to a lack of current saturation and hence a pronounced output conductance, which in turn is deleterious to the RF performance [7].

Several methods have been suggested to introduce a bandgap into graphene devices, including the use of graphene cut into the form of nanoribbons [8], graphene formed with an antidot lattice [9], and graphene in bilayers [10]. Alongside such experimental work, simulation can be used to better understand the physics of transistor operation and the limitations on transistor performance imposed by the lack of a bandgap.

Early work on the simulation of graphene-based transistors focused on nanoribbon devices (possessing a bandgap) rather than those made with wide graphene sheets (having zero bandgap), and they utilized a semiclassical top-of-the-barrier model [11]. The first quantum-mechanical simulation studies began in 2007 [12], [13], and they again focused on nanoribbon transistors; published works on the RF potential of nanoribbon FETs include those that have considered device scaling [14], [15], Schottky-barrier operation versus MOSFET-like operation [16], and bias optimization [17]. Quantum-mechanical work based on wide graphene sheets has been limited and has focused on studying pn-junctions [18] and Schottky-barrier devices [19], [20]; there has yet to be an in-depth quantum-mechanical study on the high-frequency performance of wide graphene sheets under MOSFET-like operation.

This study considers the RF potential of graphene transistors with MOSFET-like operation, with a particular focus on the absence of a bandgap. We use a fully quantum-mechanical approach to carefully describe the physics that determine the key RF metrics when there is no bandgap, including the transconductance, gate-input capacitance, and output conductance. We are also able to quantify the extent to which the lack of a bandgap limits the unity-current-gain and unity-power-gain frequencies. Our work hence allows us to provide an alternative and more detailed description of the device physics and implications of zero bandgap than recently discussed via the semiclassical approaches in [21] and [22]. Our approach is also more suited to

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[1]In this paper, we use the terms "high-frequency" and "radio-frequency" interchangeably.

study the performance potential of short-channel GFETs (having channel lengths below 20 nm) than approaches utilizing drift-diffusion models [23], [24] or Monte Carlo methods [25], since the latter methods exclude or approximate quantum-mechanical effects present in short channels. However, it should be noted that drift-diffusion and Monte Carlo approaches do have the ability to account for scattering. While scattering is most important for long channels, the inclusion of scattering in future quantum-mechanical work will be necessary to get a more complete view of the transport in short channels. Scattering effects in quantum-mechanical models have only previously been considered in the context of Schottky-barrier operation using finite-difference discretized Hamiltonians [19], [20].

Our simulations are guided by the specifications for *RF CMOS millimeter-wave (10–100 GHz) technology* in the International Technology Roadmap for Semiconductors (ITRS) for the year 2015 [26]. Of course, graphene FET fabrication techniques have yet to mature to an extent needed to achieve the ITRS requirements; we use the ITRS specifications only as a benchmark for GFET technology going forward, as we did in [27] and [28] for CNFETs. Guided by the ITRS, we employ a gate length of 18 nm and an equivalent oxide thickness (EOT) of 0.75 nm.

The simulation is carried out in two steps. First, our own self-consistent quantum-mechanical solver for GFETs (developed at the University of Alberta [29], [30]) is used to find the intrinsic characteristics of the device under ballistic conditions; we employ the method of nonequilibrium Green's functions (NEGF) together with the Poisson equation. Second, an electrostatic simulation is performed on an open-pad structure in COMSOL multiphysics [31] in order to determine the parasitic capacitances; we combine this data with theoretical values for the contact resistances in order to form an extrinsic circuit, which is then used to determine the extrinsic figures of merit.

The main outcome of our study is the extraction of both intrinsic and extrinsic RF figures of merit, together with a clear connection of their behavior to the device physics based on a fully quantum-mechanical approach. Of particular interest is the impact of a zero bandgap on the output conductance, which we show can dominate the RF behavior. Suggestions are also made for the proper biasing of graphene FETs to achieve optimum RF performance, which we show is more than adequate to keep pace with the ITRS [26], despite the lack of a bandgap.

Section II of this paper briefly outlines the simulation approach. Intrinsic results are presented in Section III, extrinsic results are presented in Section IV, and the conclusions are presented in Section V.

II. Approach

A. Device Structure

The device structure utilized for the simulations is shown in Fig. 1. Key device dimensions are indicated in the figure and Al_2O_3 (relative permittivity $\epsilon_r = 9.8$) is used as the gate oxide. The choice of Al_2O_3 is motivated by its excellent promise as a possible high-k dielectric compatible with graphene and its regular use in experimental work [32]–[34]. We use 2 nm of Al_2O_3 to replicate the ITRS EOT of 0.75 nm with SiO_2 [26]. The graphene in the source and drain regions is n-doped with a concentration $N_D = 1.9 \times 10^{17}$ m^{-2}, while the channel is left undoped; only the electron branch of the current–voltage characteristics is considered within this doping scheme.

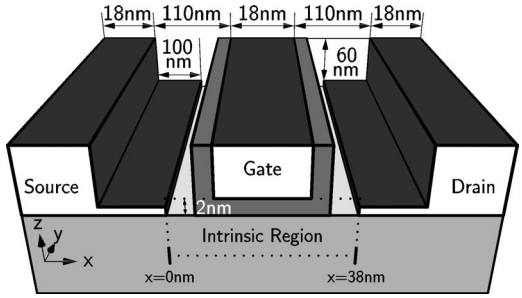


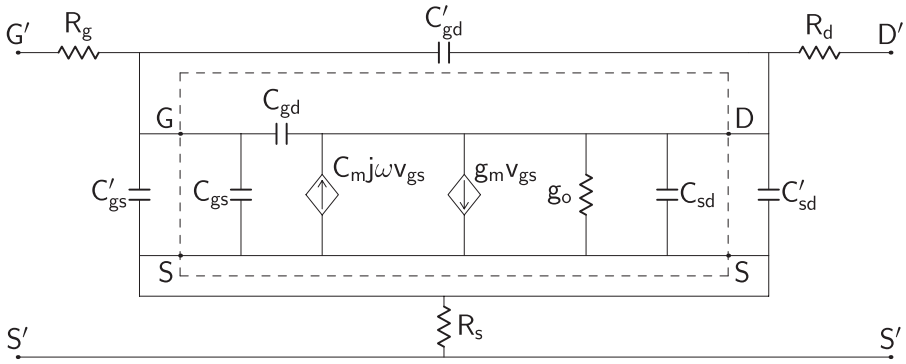
Fig. 1. Device simulated in this study. The gate length is 18 nm, and 2 nm of Al_2O_3 is used as the gate oxide. A cross section of the intrinsic region is indicated by the dotted lines. The source and drain geometries are symmetric with respect to the gate. The positions $x = 0$ and $x = 38$ nm, which delimit the intrinsic portion of the device, are labeled for later reference.

B. Intrinsic Device Simulation

1) Overview: The intrinsic simulation was carried out with our quantum-mechanical device solver applied to the dotted portion of Fig. 1. The solver computes the Poisson equation in two dimensions (along x and z) self-consistently with the NEGF formalism (along x) in order to capture both electrostatic and charge-transport effects. Simulations were carried out under ballistic conditions, which can be justified by the small gate length assumed in this study and by the aim of this paper to provide a first-order assessment and understanding of the RF capabilities of GFETs. The self-consistent solver enables the extraction of the intrinsic circuit elements, i.e., those contained within the boxed portion of Fig. 2(a); the definitions of these elements are given in Fig. 2(b) [35, Ch. 8].

2) Poisson Solver: In the same vein as the standard analysis of CMOS devices, a 2-D computational domain (along x and z) for the Poisson equation (discretized with finite differences) is used for simulating GFETs; this assumes that the potential across the graphene sheet perpendicular to the transport direction (along y) does not vary, as would be expected with an infinitely wide sheet.

3) NEGF Solver: The NEGF solver utilizes a nearest-neighbor, tight-binding Hamiltonian with a p_z-orbital basis [37]. In order to facilitate a numerical solution, Bloch boundary conditions are imposed in the direction transverse to charge transport (along y), which results in a series of orthogonal 1-D transport modes (along x). The orthogonality is ensured by the lack of scattering and the assumption of a constant potential along the width of the sheet. Numerically, the contact self-energies are calculated using the Sancho–Rubio iterative method [38], while the NEGF equations are solved utilizing the recursive Green's function technique [39] under ballistic conditions.



(a)

$$C_{gs} = -\frac{\partial q_G}{\partial v_S} \qquad C_{gd} = -\frac{\partial q_G}{\partial v_D} \qquad C_{dg} = -\chi\frac{\partial q_I}{\partial v_G}$$

$$C_m = C_{dg} - C_{gd} \qquad C_{sd} = -(1-\chi)\frac{\partial q_I}{\partial v_D}$$

$$g_o = \frac{\partial i_D}{\partial v_D} \qquad g_m = \frac{\partial i_D}{\partial v_G}$$

(b)

Fig. 2. (a) Equivalent circuit used in this study, with the intrinsic portion boxed. The labels S, D, and G refer to the source, drain, and gate terminals, respectively, of the intrinsic device, while their primed counterparts S', D', and G' refer to the corresponding extrinsic device terminals. (b) Definition of the intrinsic elements, where the symbols have their usual meanings [35, Ch. 8]. The value of the charge-partitioning factor χ has a negligible impact on the results of this paper; for completeness, we chose $\chi = 1$ based on the short length of our n^+ regions [36].

C. Extrinsic Device Simulation

To augment the intrinsic model, parasitic capacitances and contact resistances are added to the intrinsic circuit. The parasitic capacitances are found by simulating an open structure. The open structure consists of the entire device region, including the full metal contacts, but excludes the graphene sheet. The parasitic capacitances are extracted by applying a small voltage to each contact in turn and measuring the charge induced on the other contacts while the potential on the latter is held constant. COMSOL Multiphysics [31] was used to perform this task. For the contact resistances, experimental values from the literature were used. The contact resistances and parasitic capacitances were then added to the boxed portion of Fig. 2(a), yielding the overall circuit.

III. Intrinsic Results

A. Terminal Characteristics

Fig. 3 shows the intrinsic terminal characteristics of the GFET. Fig. 3(a) shows the extracted current–voltage curves, and Fig. 3(b) shows the unity-current-gain frequency f_T versus gate voltage v_G, found with the drain voltage v_D held at $V_{\rm DD}/2$ for the maximum possible signal swing at the output, where $V_{\rm DD} = 1.0$ V is used to correspond to the ITRS specification for the year 2015 [26]. Here, and elsewhere, we take the source as the reference: $v_S \equiv 0$.

The results in Fig. 3(a) depict the well-known lack of current saturation at high v_D that occurs in graphene devices and that has been observed in experiments [40]; the lack of saturation arises primarily from the lack of a bandgap and leads to an undesirably high output conductance $g_{\rm o}$.[2] Fig. 3(b) shows the f_T rising with v_G to a peak and then falling off. In what follows, we carefully explain the behavior of both $g_{\rm o}$ and f_T in graphene devices with the aid of novel expressions that shed insight into the detailed device physics. For reference, the intrinsic circuit parameter values for the device under study are provided in Table I; the values are quoted at an operating point corresponding to the peak f_T in Fig. 3(a), i.e., $v_G = 0.8$ V and $v_D = 0.5$ V, where the RF performance can be expected to be optimal.

B. Unity-Current-Gain Frequency

The unity-current-gain frequency can be written as the ratio $f_T = g_m/(2\pi C_{\rm gg})$, where g_m is the transconductance and $C_{\rm gg}$ is the capacitance seen looking into the intrinsic gate, defined as $C_{\rm gg} = \partial q_G/\partial v_G$ with v_S and v_D held constant and given by $C_{\rm gg} = C_{\rm gs} + C_{\rm gd}$ in terms of the elements in Fig. 2. The g_m and $C_{\rm gg}$ are plotted in Fig. 4.

1) Transconductance: A useful relationship for g_m (derived in the Appendix) is

$$g_m = G_0\left(1 - \frac{C_{\rm gg}}{C_{\rm ox}}\right) \times \int_{-\infty}^{\infty} \frac{\partial T(E)}{\partial E}\left[f_1(E) - f_2(E)\right] dE \tag{1}$$

where the symbols are as follows: $G_0 = 2q^2/h$ is the quantum of conductance, with q being the magnitude of the electronic charge

[2] Saturation in long-channel devices (not considered in this paper) will additionally be influenced by velocity saturation through phonon and impurity scattering [41], [42].

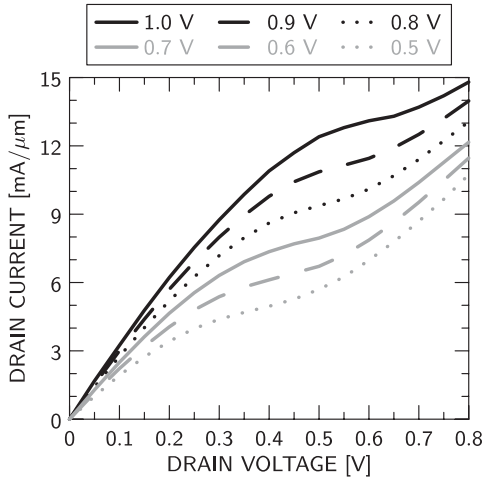


Fig. 3. Intrinsic terminal characteristics of the GFET under study, with the source used as the reference ($v_S \equiv 0$). (a) Drain current i_D versus drain voltage v_D for various values of the gate voltage v_G. (b) Unity-current-gain frequency f_T versus gate voltage v_G, found with $v_D = V_{\rm DD}/2 = 0.5$ V.

TABLE I
INTRINSIC CIRCUIT ELEMENTS AT PEAK f_T

$C_{\rm gd}$ [aF/μm]	$C_{\rm gs}$ [aF/μm]	$C_{\rm sd}$ [aF/μm]	C_m [aF/μm]	g_m [mS/μm]	$g_{\rm o}$ [mS/μm]
220	385	0	385	14.9	5.8

and h being Planck's constant; $C_{\rm ox}$ is the gate electrostatic capacitance; $T(E)$ is the total transmission function including all conducting channels; and $f_1(E)$ and $f_2(E)$ are the source and drain Fermi functions, respectively, given by

$$f_{1,2}(E) = \frac{1}{1+\exp[(E-\mu_{1,2})/k_B T_L]} \tag{2}$$

with $\mu_1 = \mu - qv_S$ being the source Fermi level, $\mu_2 = \mu - qv_D$ being the drain Fermi level, μ being the equilibrium Fermi level, k_B being Boltzmann's constant, and $T_L = 300$ K being the lattice temperature.

Since G_0 is a constant, (1) reveals that two quantities can impact the g_m. The first is the capacitance factor $(1 - C_{\rm gg}/C_{\rm ox})$,

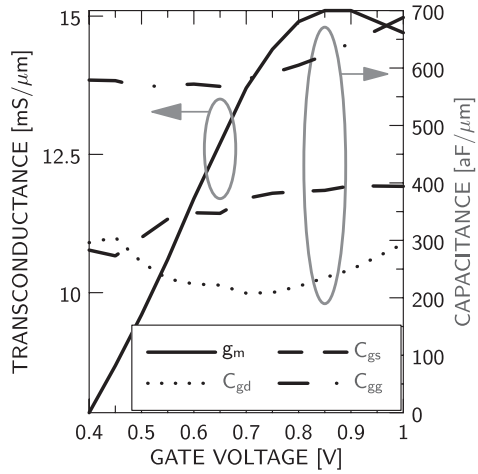


Fig. 4. Transconductance g_m and gate capacitance $C_{\rm gg}$ versus gate voltage v_G for the GFET. The components $C_{\rm gs}$ and $C_{\rm gd}$ of $C_{\rm gg}$ are also shown, where $C_{\rm gg} = C_{\rm gs} + C_{\rm gd}$. The drain voltage v_D is held fixed at $V_{\rm DD}/2 = 0.5$ V.

which represents the effectiveness of an incremental gate voltage ∂v_G in yielding an incremental change in the channel potential $\partial E_{\rm ch}$ [as shown by (19) and (27) in the Appendix]:

$$\partial E_{\rm ch} = -q\partial v_G \left(1 - \frac{C_{\rm gg}}{C_{\rm ox}}\right) \tag{3}$$

where $E_{\rm ch}$ in a graphene device (having no bandgap) can be taken to be the position of the Dirac point at the midpoint of the channel. The second is the integral, over all energies, of the responsivity in the transmission function [represented by $\partial T(E)/\partial E$] multiplied by the "difference in agenda" [43, Ch. 1] between the source and drain contacts [represented by $f_1(E) - f_2(E)$]. Overall, for a high g_m, we thus not only need the gate to effectively modulate the channel through a favorable capacitance factor $(1 - C_{\rm gg}/C_{\rm ox}) \to 1$, but also require a strong responsivity in the transmission function $\partial T(E)/\partial E$ at those energies where a nonzero difference in agenda $f_1(E) - f_2(E)$ exists.

The integral in (1) takes a particularly simple form at zero temperature, when the Fermi functions (2) reduce to step functions centered around μ_1 and μ_2

$$\int_{-\infty}^{\infty} \frac{\partial T(E)}{\partial E} \left[f_1(E) - f_2(E)\right] dE = T(\mu_1) - T(\mu_2) \tag{4}$$

which suggests that *the g_m is proportional to the difference in transmission at the source and drain Fermi levels*. While approximate, we can use this result even when $T_L \neq 0$ to qualitatively understand the bias dependence of the g_m.

First consider the three parts of Fig. 5, which show the situation in a GFET at gate and drain biases sufficient to create appreciable current; for the device under study, this corresponds to $v_G = 0.4$ V and $v_D = V_{\rm DD}/2 = 0.5$ V. Fig. 5(a) shows the spectral function (local density of states) $A(x, E)$ and the Dirac point $E_D(x)$ versus position x, Fig. 5(b) shows the spectral function $A(x, E)$ at the midpoint of the channel ($x = 19$ nm in Fig. 1) versus energy E, and Fig. 5(c) shows the corresponding transmission function $T(E)$ versus energy E. Focusing on

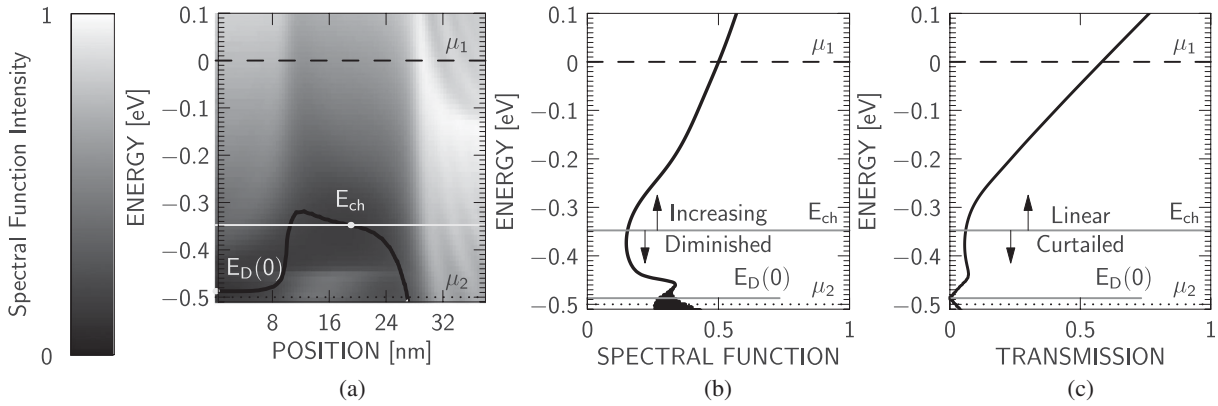


Fig. 5. Simulation results showing: (a) the spectral function $A(x, E)$ (plotted as an intensity) versus position x in the transport direction, with a superimposed sketch of the Dirac-point energy $E_D(x)$ versus x; (b) spectral function $A(x, E)$ at the midpoint of the channel ($x = 19$ nm in Fig. 1) versus energy E; and (c) the transmission function $T(E)$ versus E. Marked in the plots are the source and drain Fermi levels (μ_1 and μ_2), the channel potential $E_{\rm ch}$, and the Dirac-point energy $E_D(0)$ at the source. The results are shown for $v_G = 0.4$ V and $v_D = V_{\rm DD}/2 = 0.5$ V. For simplicity in plotting, the scaling of the spectral intensity in (a) and the scaling on the spectral and transmission axes in (b) and (c) have been normalized to unity; the values shown are hence relative, not the actual values of $A(x, E)$ and $T(E)$. For the spectral intensity, dark regions indicate a low spectral intensity, while light regions indicate a high spectral intensity.

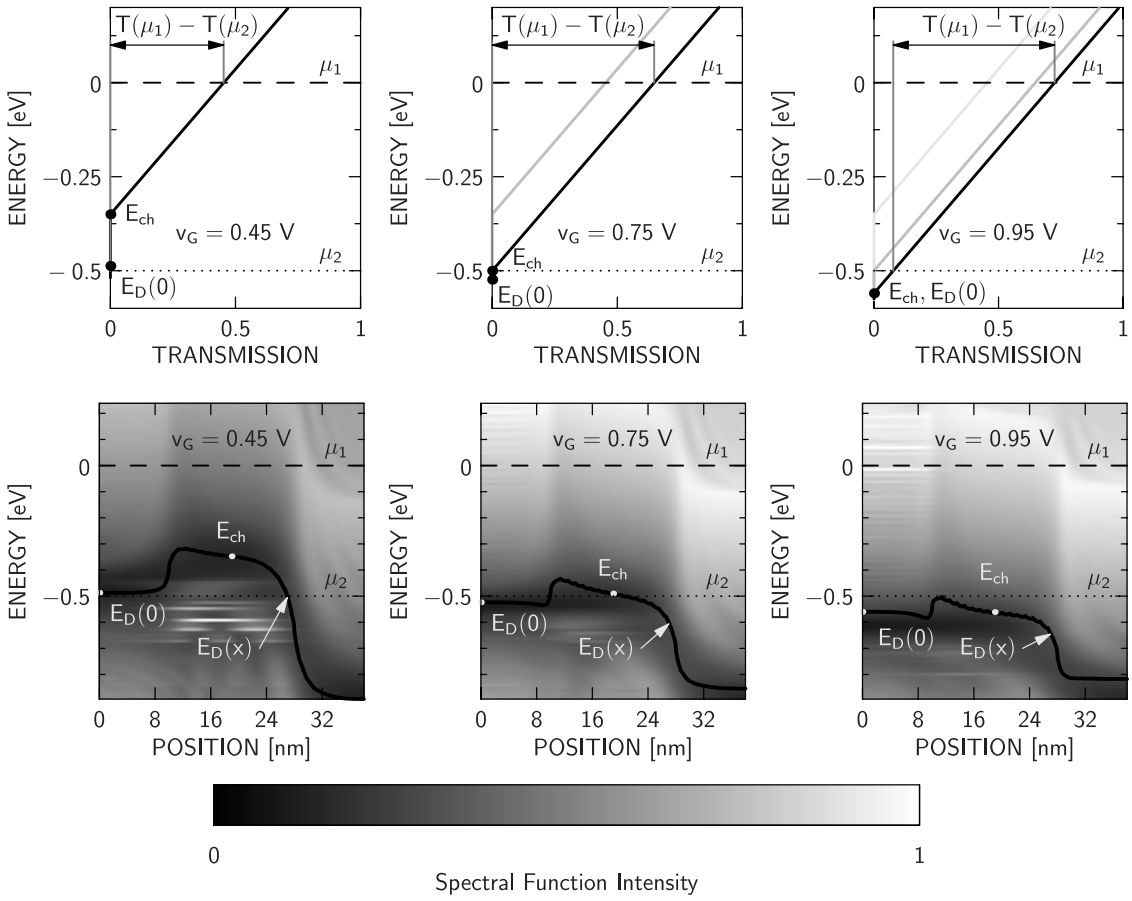


Fig. 6. Schematic illustration of the transmission function $T(E)$ versus E and corresponding sketches of the Dirac point $E_D(x)$ versus x, shown for three values of v_G, with $v_S \equiv 0$, $v_D = V_{\rm DD}/2 = 0.5$ V, and the equilibrium Fermi level $\mu \equiv 0$. The scaling on the transmission axes and of the spectral intensity has been normalized to unity; the values shown are hence relative, not the actual values of $T(E)$ and $A(x, E)$. For the spectral intensity, dark regions indicate a low spectral intensity, while light regions indicate a high spectral intensity.

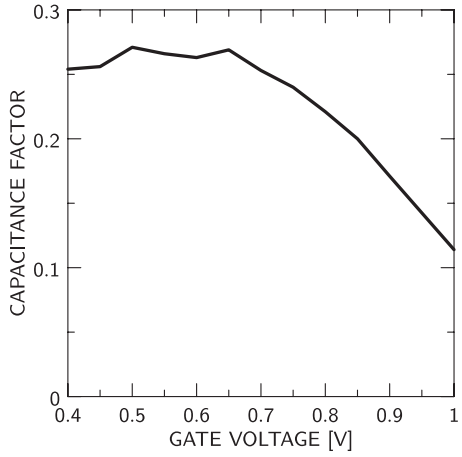


Fig. 7. Capacitance factor $(1 - C_{\rm gg}/C_{\rm ox})$ versus gate voltage v_G for the GFET. The factor appears in expression (1) for g_m.

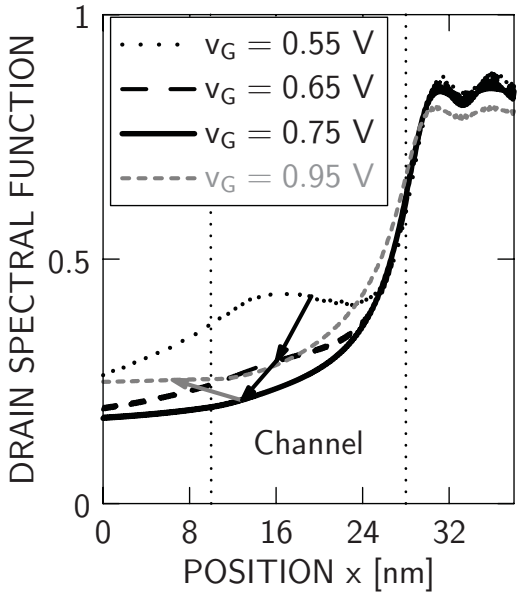


Fig. 8. Drain spectral function (local density of states that can be filled by the drain) evaluated at the drain Fermi level μ_2 and plotted versus position x, i.e., $A_D(x, \mu_2)$ versus x. Curves are shown for several values of the applied gate voltage v_G. The black arrows indicate the shift in the spectral function as the gate voltage is increased, until the spectral function reaches its minimum value in the channel at $v_G = 0.75$ V; the gray arrow then indicates the upward shift in the spectral function as the gate voltage is further increased (beyond $v_G = 0.75$ V). The scaling on the spectral axis has been normalized to unity for plotting purposes.

Fig. 5(a) and (b), it is evident that the number of states available for transport increases with energy E for $E \geq E_{\rm ch}$ and is diminished for energies $E_D(0) \leq E \leq E_{\rm ch}$, where the latter can be attributed to the potential barrier depicted by the shape of $E_D(x)$. In graphene, this yields a transmission $T(E)$ that increases linearly for energies $E \geq E_{\rm ch}$ and which is curtailed for $E_D(0) \leq E \leq E_{\rm ch}$, as shown in Fig. 5(c). It is worth mentioning that the asymmetry in states [and hence $T(E)$] about $E_{\rm ch}$ is unique to our quantum-mechanical approach; semiclassical top-of-the-barrier models, such as those in [21] and [22], effectively assume a symmetrical distribution of states (and hence transmission) about $E_{\rm ch}$.

As the gate voltage is increased, the entire picture in Fig. 5 can be visualized as being "pushed down." We have illustrated the situation schematically in the three parts of Fig. 6, shown for $v_G = 0.45, 0.75$, and 0.95 V, using a linear form for $T(E)$ for $E \geq E_{\rm ch}$ and $T(E) \approx 0$ for $E_D(0) \leq E \leq E_{\rm ch}$; we have also sketched the difference $T(\mu_1) - T(\mu_2)$ that impacts the g_m according to (4). Initially, $T(\mu_1)$ increases with v_G, while $T(\mu_2) \approx 0$; at $v_G = 0.75$ V, the channel potential has been sufficiently pushed down to be aligned with μ_2, and for higher v_G, μ_2 moves into the range of energies corresponding to the linearly increasing portion of $T(E)$, such that the difference $T(\mu_1) - T(\mu_2)$ saturates. These observations are consistent with the behavior of g_m in Fig. 4, which shows that g_m increases with applied gate voltage and then begins to saturate for $v_G \geq 0.75$ V.

The eventual slight decrease in g_m for $v_G \geq 0.9$ V can be attributed to the capacitance factor $(1 - C_{\rm gg}/C_{\rm ox})$ appearing in (1). This factor is plotted in Fig. 7; at sufficiently high gate voltages ($v_G \geq 0.75$ V), the factor experiences a noticeable decline, which begins to dominate the behavior of the g_m. Since $C_{\rm ox}$ is a constant (having no dependence on the bias point), the decline is due to a rising $C_{\rm gg} = C_{\rm gs} + C_{\rm gd}$, which occurs because the GFET enters an "ohmic" regime of operation, as we will describe in the next section.

Overall, the results in Figs. 4–7, along with the expressions (1) and (4), indicate that *the g_m in a graphene device can be expected to increase with gate voltage and eventually saturate (or peak) when v_G is chosen such that the drain Fermi level aligns with the channel potential: $\mu_2 = E_{\rm ch}$.*

2) Gate Capacitance: As shown in Fig. 4, the gate–drain capacitance $C_{\rm gd}$ exhibits a definite minimum at $v_G = 0.75$ V, while the gate–source capacitance $C_{\rm gs}$ is approximately constant for $v_G \geq 0.75$ V. Much of the rise in the input capacitance $C_{\rm gg} = C_{\rm gs} + C_{\rm gd}$ for $v_G \geq 0.75$ V can thus be attributed to the corresponding rise in $C_{\rm gd}$.

$C_{\rm gd}$ can be written in terms of the physics-based capacitances in Fig. 12 of the Appendix:

$$C_{\rm gd} = \frac{C_{\rm ox}(C_{\rm de} + C_{\rm dq})}{C_{\rm ox} + C_{\rm se} + C_{\rm sq} + C_{\rm de} + C_{\rm dq}}. \tag{5}$$

Its behavior can then be understood by considering the plots of $E_D(x)$ versus x in Fig. 6 along with the results in Fig. 8, where the latter shows the drain spectral function (local density of states that can be filled by the drain) evaluated at an energy equal to the drain Fermi level μ_2 and plotted versus position x, i.e., $A_D(x, \mu_2)$ versus x. For gate biases below the minimum of the $C_{\rm gd}$ curve in Fig. 4, the drain Fermi level in Fig. 6 is well below the channel potential $E_{\rm ch}$, and a relatively high density of states in equilibrium with μ_2 is available at the midpoint of the channel ($x = 19$ nm in Fig. 1), as shown, for example, by the curve for $v_G = 0.55$ V in Fig. 8. As the gate voltage increases and $E_D(x)$ is pushed down, Fig. 6 illustrates that the drain Fermi level μ_2 moves up with respect to $E_{\rm ch}$ and eventually aligns with it. Correspondingly, in Fig. 8, as v_G is varied from 0.55 to 0.75 V, the available density of states at $E = \mu_2$ at the midpoint of the

channel falls, reaching a minimum at $v_G = 0.75$ V. Since the drain quantum capacitance $C_{\rm dq}$ depends directly on the available density of states at the drain Fermi level [43, Ch. 7], it will follow the same trend; $C_{\rm dq}$ will fall from its value at $v_G = 0.55$ V to a minimum at $v_G = 0.75$ V. Given $\partial C_{\rm gd}/\partial C_{\rm dq} > 0$ according to (5), the fall in $C_{\rm dq}$ has the effect of reducing $C_{\rm gd}$ until $v_G = 0.75$ V, as illustrated in Fig. 4.

Further increases in v_G beyond 0.75 V cause μ_2 to be positioned above $E_{\rm ch}$, as shown, for example, by the results for $v_G = 0.95$ V in Fig. 6. The device now enters an "ohmic" region of operation, where both Fermi levels are positioned above the Dirac point $E_D(x)$ for all x, and the transport becomes indistinguishable from that in a metallic conductor with a linear potential profile (versus x) and an applied voltage $v = (1/q)(\mu_1 - \mu_2)$; note that by "ohmic," we refer only to the metallic nature of the potential profile, not the "ohmic" or "triode" region of textbook FET operation. As a result, the drain terminal can be expected to gain increased control over the channel potential $E_{\rm ch}$, which is equivalent to suggesting that the capacitance $C_D = C_{\rm de} + C_{\rm dq}$ associated with the drain in Fig. 12 increases, and hence that $C_{\rm gd}$ in (5) increases, as illustrated in Fig. 4.

3) Bias Point for Peak f_T: Based on the discussion of g_m and $C_{\rm gg}$, it becomes evident that *the peak f_T will be achieved when the gate bias is chosen to align the drain Fermi level with the channel potential*

$$\boxed{\mu_2 = E_{\rm ch}.} \tag{6}$$

This bias point will maximize the transconductance g_m while keeping the gate capacitance $C_{\rm gg}$ from increasing due to ohmic operation, yielding an optimum $f_T = g_m/(2\pi C_{\rm gg})$. For the device under study, $\mu_2 = E_{\rm ch}$ is achieved for $v_G = 0.75$ V, which corresponds to the peak in the f_T curve of Fig. 3(b).

C. Output Conductance

1) Expression: A useful expression for the output conductance can be found by following steps similar to those in the Appendix leading to (1) for the transconductance.

The output conductance is defined as

$$g_{\rm o} = \frac{\partial i_D}{\partial v_D} \tag{7}$$

where the derivative is to be evaluated while holding the gate and source voltages (v_G and v_S) constant. Differentiating (20) for the current while using the product rule and the fact that the source Fermi function $f_1(E)$ in (2) has no dependence on v_D, we find

$$\frac{\partial i_D}{\partial v_D} = \frac{2q}{h}\int_{-\infty}^{\infty}\left\{\frac{\partial T(E)}{\partial v_D}\left[f_1(E) - f_2(E)\right] - T(E)\frac{\partial f_2(E)}{\partial v_D}\right\} dE. \tag{8}$$

This expression suggests the output conductance can be written as the sum of two components

$$\boxed{g_{\rm o} \equiv \frac{\partial i_D}{\partial v_D} \equiv g_{\rm ob} + g_{\rm oq}} \tag{9}$$

where

$$g_{\rm ob} \equiv \frac{2q}{h}\int_{-\infty}^{\infty}\frac{\partial T(E)}{\partial v_D}\left[f_1(E) - f_2(E)\right] dE \tag{10}$$

and

$$g_{\rm oq} \equiv \frac{2q}{h}\int_{-\infty}^{\infty} -T(E)\frac{\partial f_2(E)}{\partial v_D}\, dE = \frac{2q^2}{h}\int_{-\infty}^{\infty} T(E)\frac{\partial f_2(E)}{\partial E}\, dE. \tag{11}$$

2) Interpretation: The component $g_{\rm oq}$ in (11) is best understood at zero temperature. The derivative of the Fermi function will become a Dirac-delta function centered at the drain Fermi level μ_2. Performing the integration in (11) then reveals

$$\boxed{g_{\rm oq} = G_0 T(\mu_2)} \tag{12}$$

which highlights the interpretation of $g_{\rm oq}$ as an *output conductance component due to quantum-mechanical transmission around the drain Fermi level*.

The component $g_{\rm ob}$ in (10) represents the effects of *conventional drain-induced barrier lowering* (DIBL), which can be understood with the aid of Fig. 12. With $C_D \equiv C_{\rm de} + C_{\rm dq}$, the incremental channel potential due to the application of an incremental drain voltage $-q\partial v_D$ (with the gate and source voltages held constant) is given by

$$\partial E_{\rm ch} = -q\partial v_D \frac{C_D}{C_T} = -q\partial v_D \frac{C_{\rm gd}}{C_{\rm ox}} \tag{13}$$

where C_T is the total capacitance in Fig. 12, as specified below (19) in the Appendix, and where the relation $C_D/C_T = C_{\rm gd}/C_{\rm ox}$ follows from (5). Using steps similar to those in the Appendix, one then obtains

$$\boxed{g_{\rm ob} = G_0 \frac{C_{\rm gd}}{C_{\rm ox}}\int_{-\infty}^{\infty}\frac{\partial T(E)}{\partial E}\left[f_1(E) - f_2(E)\right] dE.} \tag{14}$$

The interpretation of (14) is hence similar to (1), with the only difference being in the capacitive factor multiplying the integral; in the present case of (14), this factor reflects the direct control of an incremental drain voltage ∂v_D over an incremental channel potential $\partial E_{\rm ch}$ according to (13), and hence the control of ∂v_D over the source-to-drain barrier height and the incremental drain current ∂i_D.

3) Relation to Traditional MOSFETs: The aforementioned results (12) and (14) can also be interpreted in the context of traditional (silicon) MOSFETs versus graphene.

In a traditional semiconductor possessing a bandgap, we find that transmission around the drain Fermi level is impossible, i.e., $T(\mu_2) = 0$; this follows from the fact that under normal operating conditions, the drain Fermi level is located at an energy that falls within the bandgap of the energy-band profile of a traditional device channel, such that very little transmission can occur. As a result, for a traditional semiconductor, we find $g_{\rm oq} = 0$ from (12). On the other hand, this result does not necessarily apply to graphene, which possesses no bandgap.

Regarding the component $g_{\rm ob}$ in (14), in conventional transistors with a bandgap, the control of the drain on the channel

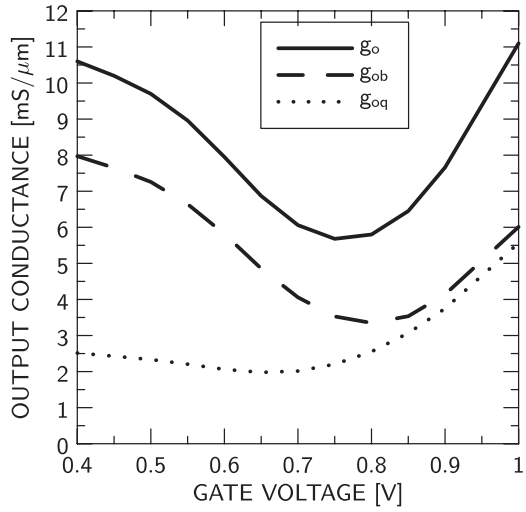


Fig. 9. Output conductance $g_{\rm o}$ and its components $g_{\rm ob}$ and $g_{\rm oq}$ versus gate voltage v_G for the GFET. The drain voltage is held at $v_D = V_{\rm DD}/2 = 0.5$ V.

region (indicated by the factor $C_{\rm gd}/C_{\rm ox}$) under normal operating conditions is limited to conventional electrostatic DIBL, i.e., the ratio $C_{\rm gd}/C_{\rm ox}$, which was specified earlier in (5), is determined only by $C_{\rm de}$ in the numerator, with $C_{\rm dq} \to 0$; in the absence of conventional DIBL, we also have $C_{\rm de} \to 0$, and we hence find $g_{\rm ob}$ in (14) can be made to vanish in a traditional device. On the other hand, this outcome cannot be made to occur in graphene, due to a pronounced $C_{\rm dq}$ arising from the lack of a bandgap, where the behavior of $C_{\rm dq}$ was already discussed in conjunction with (5) and Fig. 8.

4) Results: Values for the output conductance $g_{\rm o}$ and its components $g_{\rm ob}$ and $g_{\rm oq}$ [computed from (10) and (11)] versus gate voltage v_G are displayed in Fig. 9, and they can easily be understood by appealing to the results already discussed.

The component $g_{\rm oq}$ exhibits a weak minimum at $v_G = 0.75$ V, where the drain Fermi level μ_2 aligns with the channel potential $E_{\rm ch}$ (see Fig. 6). At this point, $T(\mu_2)$ is minimized, which has the effect of minimizing $g_{\rm oq}$ as suggested by (12); for gate voltages beyond this point, μ_2 moves into the linear portion of $T(E)$ (see Fig. 6), causing $g_{\rm oq}$ to rapidly increase, as illustrated in Fig. 9.

The component $g_{\rm ob}$ exhibits a well-defined minimum at $v_G \approx 0.75$ V. To first order, this corresponds to the behavior of $C_{\rm gd}$, which dominates the behavior of $g_{\rm ob}$ through the ratio $C_{\rm gd}/C_{\rm ox}$ appearing in (14), where $C_{\rm ox}$ is a constant; as discussed earlier and as illustrated in Fig. 4, $C_{\rm gd}$ will exhibit a minimum at $v_G = 0.75$ V, where $\mu_2 = E_{\rm ch}$.

Overall, the results in Fig. 9 show that both the components $g_{\rm oq}$ and $g_{\rm ob}$ are minimized when the biasing is chosen such that $\mu_2 = E_{\rm ch}$, the same condition identified earlier as yielding peak f_T. It is worth mentioning that these observations elaborate on those made in [21] and [22]. The approach in [21] is equivalent to assuming $g_{\rm o} = g_{\rm oq}$, and the authors point out that the condition $\mu_2 = E_{\rm ch}$ will ideally yield $g_{\rm o} = g_{\rm oq} = 0$ [21, Fig. 2]; a strong minimum in $g_{\rm oq}$ is also observed in [21], rather than the weak minimum shown here in Fig. 9, which can be attributed to the missing asymmetry in $T(E)$ in [21]. In [22], it is suggested that the lack of a bandgap can cause $C_{\rm dq}$ and hence $C_{\rm gd}$ to be appreciable, and that this can impact the high-frequency performance [22, eq. (28)], which is equivalent to considering the impact of $g_{\rm ob}$. Our approach naturally identifies and clarifies the role of both components.

TABLE II
RF METRICS

	Power Supply Voltage $V_{\rm DD}$ [V]	**Gate Length L_g [nm]**	**Peak f'_T [GHz]**	**Peak $f_{\rm max}$ [GHz]**	**MSG/ MAG [dB] at 24 GHz**	**MSG/ MAG [dB] at 60 GHz**	**MSG/ MAG [dB] at 94 GHz**
GFET in this paper	1.0	18	2700	3000	31.4	20.5	18.5
RF CMOS (ITRS) [26]	1.0	18	490	560	17.9	13.9	11.9

IV. EXTRINSIC RESULTS

As mentioned in Section II, COMSOL was used to calculate the parasitic capacitances, with the device width set equal to 1 μm (for demonstration purposes); values of $C'_{\rm sd} = 24$ aF, $C'_{\rm gd} = 40$ aF, and $C'_{\rm gs} = 40$ aF were obtained for the GFET structure of Fig. 1. The source and drain contact resistances were taken to be $R_S = R_D = 50\,\Omega$, near the theoretical minimum for graphene [44], [45]. While these values may be viewed as optimistic, they are consistent with our aim of performing a best-case assessment and should be achievable with improvements in the fabrication process; moreover, we have found that the important outcomes of the results presented here (on the impact of a lack of a bandgap and correspondingly high $g_{\rm o}$ on the RF metrics) are not affected by the specific values chosen. For the gate resistance, we used a value $R_{\rm g,eff} = 220/3\Omega$, which can be calculated by considering a tungsten gate contact of dimensions $W_g \times L_g \times t_g = 1\,\mu{\rm m} \times 18\,{\rm nm} \times 60\,{\rm nm}$; this material was chosen due to the match in the work function with graphene. These parasitics were used in conjunction with the circuit in Fig. 2 to determine the extrinsic figures of merit.

A. RF Metrics

Table II presents several key RF metrics for the GFET, including the extrinsic unity-current-gain frequency f'_T, the unity-power-gain frequency $f_{\rm max}$, the maximum available gain (MAG) [46], and the maximum stable gain (MSG $= |y_{21}/y_{12}|$, where y_{21} and y_{12} refer to the forward and reverse transadmittances, respectively). The $f_{\rm max}$ was found by extrapolating Mason's unilateral gain (U) [47] to unity at -20 dB/decade.

Since the GFET values in Table II are based on the assumption of ballistic transport, they can be interpreted as indicating that GFETs have ample potential to meet the requirements of the ITRS [26] going forward, and that this potential can be realized despite the lack of a bandgap and the ensuing lack of current saturation [see Fig. 3(a)], which leads to a poor output conductance $g_{\rm o}$. We will elaborate further on this point by quantifying the precise impact of $g_{\rm o}$ on the attainable f'_T and $f_{\rm max}$.

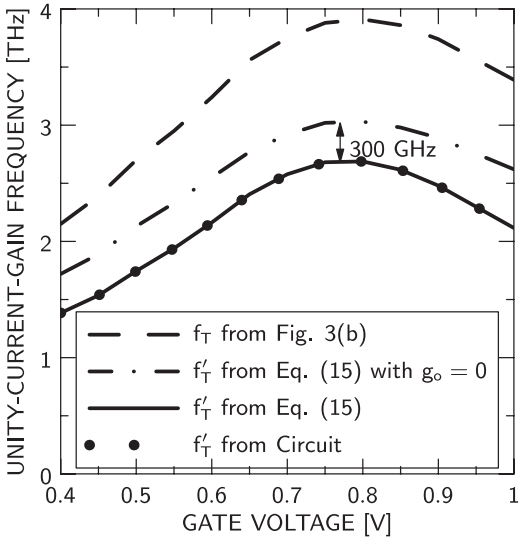


Fig. 10. Extrinsic unity-current-gain frequency f'_T versus gate voltage v_G as found from (15). Values of f'_T extracted from the circuit of Fig. 2 are also shown to validate (15), and values of the *intrinsic* f_T reproduced from Fig. 3(b) are shown for reference.

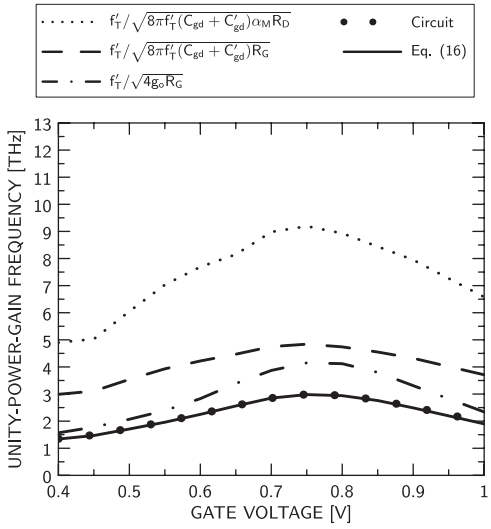


Fig. 11. Plot of the components of the unity-power-gain frequency $f_{\max}$ according to the expression (16) versus gate voltage v_G. Values of $f_{\max}$ obtained from the circuit of Fig. 2 are also shown to validate (16).

B. Unity-Current-Gain Frequency

An expression for the extrinsic unity-current-gain frequency that includes the effects of output conductance is [48]

$$f'_T \approx \frac{f_T}{\alpha_T + [\alpha_T g_o + 2\pi f_T (C_{gd} + C'_{gd})]\,(R_S + R_D)} \quad (15)$$

where $\alpha_T \equiv (C_{gg} + C'_{gs} + C'_{gd})/C_{gg}$. Fig. 10 shows a plot of (15) with and without g_o, along with results from the circuit of Fig. 2, which are used to validate (15). As shown, the impact of a nonzero g_o in graphene is to reduce the peak f'_T by about 300 GHz; the overall impact of the lack of a bandgap is actually greater, since it also leads to a higher C_{dq} and hence higher C_{gd} [as discussed in conjunction with (5)], increasing the importance of the term involving R_S and R_D in (15).

C. Unity-Power-Gain Frequency

An expression for $f_{\max}$ that includes the effect of output conductance is [48]

$$f_{\max} \approx \frac{f'_T}{\sqrt{4g_o R_G + 8\pi f'_T (C_{gd} + C'_{gd})\,[R_G + \alpha_M R_D]}} \quad (16)$$

where

$$\alpha_M \equiv \frac{C_{gd} + C'_{gd} + C_{sd} + C'_{sd}}{C_{gg} + C'_{gs} + C'_{gd}}. \quad (17)$$

Fig. 11 shows a plot of the components on the right-hand side of (16), along with results from the circuit of Fig. 2. When all three terms in the denominator of (16) are included, the agreement with the results from the circuit is nearly perfect, which validates the expression. The impact of the term involving the drain resistance R_D is secondary, with the associated values $f'_T/\sqrt{8\pi f'_T (C_{gd} + C'_{gd})\alpha_M R_D}$ greatly exceeding the true $f_{\max}$. Retaining only the term involving R_G and C_{gd} yields the classical expression $f'_T/\sqrt{8\pi f'_T (C_{gd} + C'_{gd}) R_G}$ for the $f_{\max}$ of RF transistors [35, Ch. 8], [49]; however, as shown, this overestimates the true peak $f_{\max}$ by close to a factor of 2. The reduction is primarily due to the output conductance g_o, with the associated values $f'_T/\sqrt{4g_o R_G}$ providing the closest estimate to the true $f_{\max}$. These results, which are founded on our fully quantum-mechanical simulations, thus suggest that the lack of a bandgap, and the associated poor output conductance, limits the RF potential of graphene (as measured by peak $f_{\max}$) by approximately a factor of 2. While the data in Table II show that graphene should nevertheless be competitive, the results in Fig. 11 suggest that it is worthwhile to pursue modified forms of graphene exhibiting a bandgap and better output conductance to further improve the high-frequency performance.

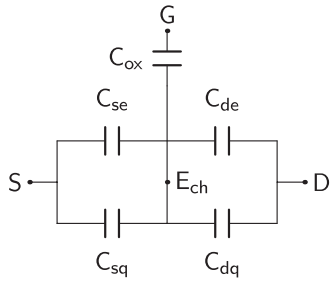


Fig. 12. Equivalent circuit between the external terminals and the channel as derived from a general theory of ballistic nanotransistors [50], [51].

V. Conclusion

The following conclusions can be drawn from this study on the impact of a zero bandgap on the RF potential of GFET transistors.

1) Based on ballistic quantum-mechanical transport in the intrinsic device, the lack of a bandgap causes optimum RF performance to be realized under the bias condition

where the drain Fermi level μ_2 aligns with the channel potential $E_{\rm ch}$, as specified by (6).

2) This bias point, which corresponds to $v_G \sim 0.75$ V (where $v_D \equiv V_{\rm DD}/2 = 0.5$ V) for the chosen device, yields an optimum transconductance g_m while keeping the gate–drain capacitance $C_{\rm gd}$ and hence the input capacitance $C_{\rm gg}$ from increasing due to "ohmic" operation, thus yielding an optimum intrinsic $f_T = g_m/(2\pi C_{\rm gg})$ [see Figs. 3(b) and 4].
3) The same bias point leads to an optimum value for the intrinsic output conductance $g_{\rm o}$, which can be viewed as being comprised of two parts: a quantum component $g_{\rm oq}$ and a conventional DIBL component $g_{\rm ob}$. The relevant equations revealing the associated physics are (9), (12), and (14), and the relevant figure illustrating the behavior of $g_{\rm o}$ is Fig. 9.
4) The relatively poor output conductance limits the extrinsic f_T' and $f_{\rm max}$, a feature which is unique to graphene transistors. With the aid of (15) and (16), our fully quantum-mechanical simulations suggest the peak f_T' could be increased by 300 GHz and the peak $f_{\rm max}$ could be doubled (see Figs. 10 and 11) if a bandgap could be introduced to cause $g_{\rm o} \to 0$ while leaving all other parameters unchanged.

Despite the lack of a bandgap and a pronounced output conductance, our results show that graphene transistors exhibit more than sufficient potential to keep pace with ITRS [26] requirements (see Table II). Further studies on the effects of phonon scattering and the effects of introducing a bandgap are warranted to get a more complete description of the RF potential of graphene devices.

APPENDIX

DERIVATION OF THE EXPRESSION FOR TRANSCONDUCTANCE

The transconductance is defined as

$$g_m = \frac{\partial i_D}{\partial v_G} \tag{18}$$

where the derivative is to be evaluated with the source and drain voltages (v_S and v_D) held constant.

To find an expression for the derivative, we first refer to the circuit of Fig. 12, which can be derived from a general theory of ballistic nanotransistors [50], [51]. The circuit allows a computation of the channel potential $E_{\rm ch}$ (expressed in the units of electron energy) in terms of the external voltages and physics-based capacitances in the device, where for graphene devices, as mentioned in Section III, the channel potential can be taken to be the position of the Dirac point at the midpoint of the channel. The capacitances in the circuit are the gate electrostatic (oxide) capacitance ($C_{\rm ox}$), the drain electrostatic and quantum capacitances ($C_{\rm de}$ and $C_{\rm dq}$), and the source electrostatic and quantum capacitances ($C_{\rm se}$ and $C_{\rm sq}$).

From the circuit of Fig. 12, we can write the incremental channel potential $\partial E_{\rm ch}$ that arises from an incremental gate voltage ∂v_G (with $\partial v_S = \partial v_D = 0$) as follows:

$$\partial E_{\rm ch} = -q\partial v_G \frac{C_{\rm ox}}{C_T} \tag{19}$$

where $C_T = C_{\rm de} + C_{\rm dq} + C_{\rm se} + C_{\rm sq} + C_{\rm ox}$ is the algebraic sum of all the capacitances in Fig. 12 and facilitates a convenient shorthand when expressing the result of the voltage division.

From the NEGF (or Landauer) formalism, the current is [37, p. 321]

$$i_D = \frac{2q}{h}\int_{-\infty}^{\infty} T(E)\left[f_1(E) - f_2(E)\right]\,dE. \tag{20}$$

Equation (20) can be differentiated with respect to the channel potential while holding the source and drain voltages constant; this means that the Fermi functions [specified by (2)] will be unaffected by the differentiation, which will therefore impact only the transmission function. Performing the operation, we find

$$\frac{\partial i_D}{\partial E_{\rm ch}} = \frac{2q}{h}\int_{-\infty}^{\infty} \frac{\partial T(E)}{\partial E_{\rm ch}}\left[f_1(E) - f_2(E)\right]\,dE \tag{21}$$

which combined with (19) then yields

$$\frac{\partial i_D}{\partial v_G} = -\frac{2q^2}{h}\frac{C_{\rm ox}}{C_T}\int_{-\infty}^{\infty} \frac{\partial T(E)}{\partial E_{\rm ch}}\left[f_1(E) - f_2(E)\right]\,dE. \tag{22}$$

As a first approximation, the *shape* of the transmission function remains fixed under a perturbation, such that an incremental change $\partial E_{\rm ch}$ in the channel potential simply *shifts* the function: $T(E) \to T(E - \partial E_{\rm ch})$. The change in the transmission $\partial T(E)$ at an energy E from the shift can then be written as a difference equation

$$\partial T(E) = T(E - \partial E_{\rm ch}) - T(E) \tag{23}$$

from which

$$\partial T(E) = \frac{\partial T(E)}{\partial E}(-\partial E_{\rm ch}) \tag{24}$$

or

$$\frac{\partial T(E)}{\partial E_{\rm ch}} = -\frac{\partial T(E)}{\partial E}. \tag{25}$$

Substituting the relationship (25) into (22) then gives

$$g_m = \frac{2q^2}{h}\frac{C_{\rm ox}}{C_T}\int_{-\infty}^{\infty} \frac{\partial T(E)}{\partial E}\left[f_1(E) - f_2(E)\right]\,dE \tag{26}$$

which can be recast into the final form (1) by recognizing that the circuit of Fig. 12 implies

$$\frac{C_{\rm ox}}{C_T} = \left(1 - \frac{C_{\rm gg}}{C_{\rm ox}}\right) \tag{27}$$

and that $G_0 \equiv 2q^2/h$.

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